Air Cooled SiC Three Level Inverter Reaches Efficiency Levels Above 99 Percent

Power Electronics Europe has sponsored the Best Paper Award of PCIM Europe 2017. At Siemens a dual three-phase 3-level inverter (2 x 27 kW; input 600 VDC; output 2 x 400 VAC 45 Arms) has been realized with the latest generation of planar SiC-MOSFETs, a space saving embedding technology of power semiconductors, an optimized air cooling concept and a novel DC link configuration. The inverter has a high power density of 17,2 kW/l combined with an efficiency of 99,2 percent. With the new design the volume could be reduced by a factor of six in comparison to a standard high-performance Si-based converter. These features convinced the award committee to give the award to **Alexander Hensler, Siemens AG, Nuremberg, Germany**

Silicon Carbide (SiC) power devices have been significantly improved over the recent years. Especially the developments of 1200 V SiC MOSFETs are remarkable. These wide bandgap devices, combined with an optimized inverter design, enable new breakthroughs in power density and performance. Silicon-based devices with their bipolar behavior such as IGBTs have drawbacks due to the threshold voltage in the output characteristics (Figure 1) and much higher switching losses in comparison to SiC MOSFETs. For the assumption of 1 V voltage drop and typical switching losses of 50 %, maximum efficiency of about 99 % is reachable with 1200 V devices.

However, improvements of a drive application cannot be reached only by a replacement of Si devices with the new SiC MOSFETs. Especially, the fast switching of SiC devices requires a new approach of packaging and interconnection technology. A low inductive design is necessary to keep over-voltage and EMI low at high switching transients. Further aspects, such as inverter topology, cooling concept, gate drivers and power supplies have to be considered and optimized for SiC power devices. A new holistic approach for the inverter design can contribute remarkably to higher power density.

SiC inverter topology

Considering the electrical properties of SiC MOSFETs and a system benefit for the whole inverter, a dual T-type three level topology was chosen, as shown in Figure 2. Two 3-phase inverters enable AC/AC operation. For DC/AC purposes, two inverters can be used for double-axis drive applications. Additionally, with a parallel connection of two inverters using external inductances, a higher output current is possible. Often, there are discussions whether a three level topology for SiC MOSFETs is reasonable. With much lower switching losses, the switching frequency can be increased and therefore improvements in comparison to a Si-based inverter are achievable.

Considering optional filtering, a three level inverter delivers additional improvements. Since the inverter design should cover the possibility of a drive solution with a filter for a pure sine output voltage, the T-type three level topology was chosen as the preferred solution.

The low switching losses of SiC MOSFETs combined with the advantages of a three level topology, a switching frequency of up to 100 kHz is reachable with acceptable switching losses. Under these conditions, an inverter solution towards ideal pure sinusoidal output voltage with a high power density is achievable, which corresponds with an evaluation of different topologies to Google's little box challenge.

PCB-based half bridge

The whole converter consists of six half bridges. Each half-bridge (Figure 3) is

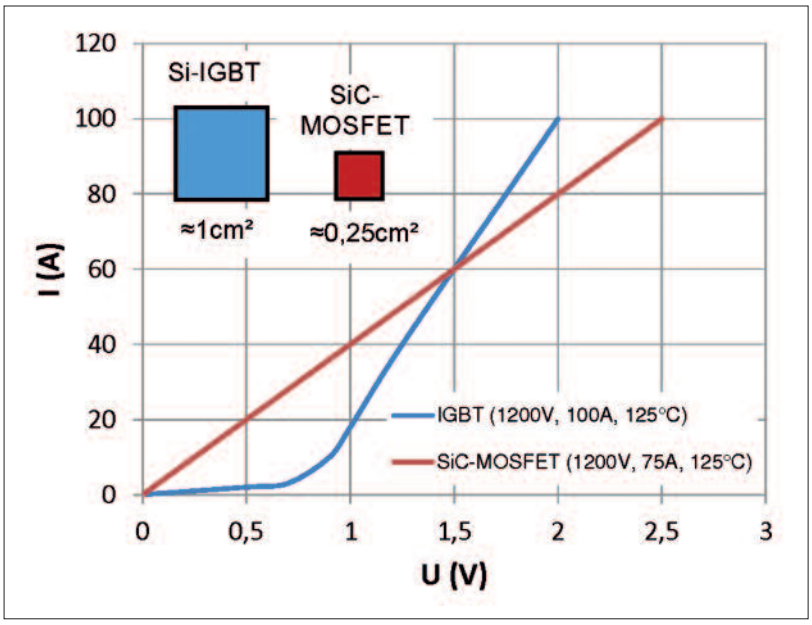

Figure 1: Output characteristics of IGBT and SiC MOSFET and comparison of chip area

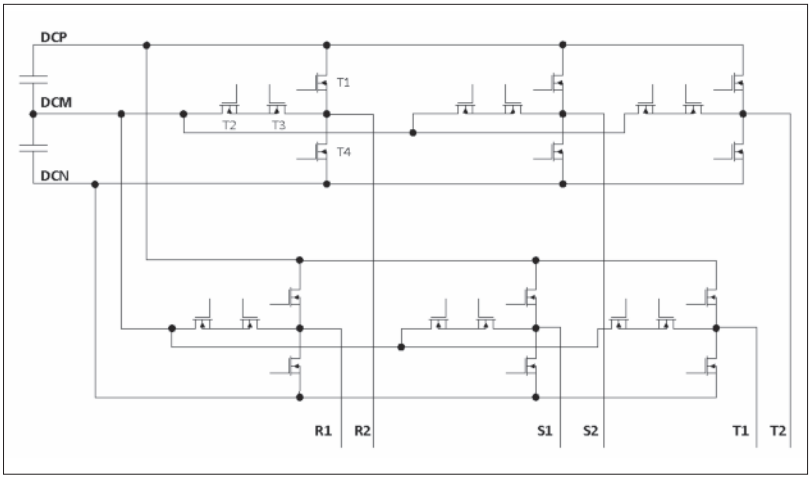

Figure 2: **Dual T-type topology with SiC MOSFETs**

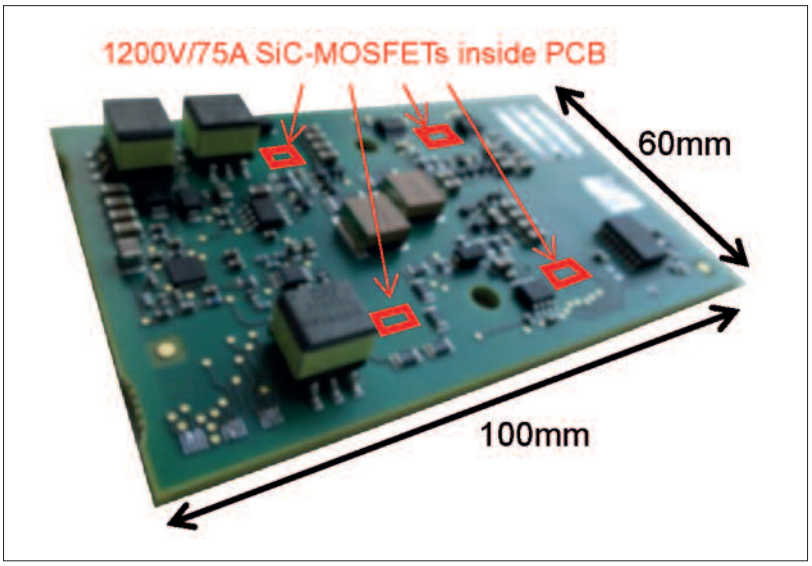

Figure 3: **PCB-based half bridge with four embedded SiC MOSFETs and integrated functions**

realized with a multilayer printed circuit board (PCB). On the top side, there are three isolated auxiliary power supplies, gate drivers and measurement circuits for output current and output voltage. One half bridge has an additional measurement circuit for the two DC link voltages. For the current measurement, an isolated sensor, based on the magneto resistive principle, is utilized. Each PCB carries a part of the DC link capacitanc in form of a snubber capacitor (CeraLink™). Furthermore, on each PCB a temperature sensor is placed near to the hottest spot.

Inside the PCB, four SiC MOSFETs are embedded. All four power semiconductors of the half bridges are 1200V/75A devices. For the middle switch, between the midpoint of the DC link and the AC output of the inverter, two 650 V SiC MOSFETs would be sufficient, but were not implemented in favor for a simplification of the prototype design. There are no external parallel freewheeling diodes - the intrinsic body diode of the SiC MOSFET is used for inverter operation.

With a multilayer layer PCB a low inductive commutation circuit has been realized for the switching events between the SiC MOSFETs and the CeraLink capacitors. The main DC link capacitance is located externally and is not a part of the half bridge. On the bottom side of the PCB a thermal interface to the heat sink is provided. Also the interface to a control board is located on the bottom side.

Optimized cooling concept

The optimized cooling solution has the shape of a hexagon, the six half bridge PCBs are located with the thermal interface facing the flattened heat sink area. The fins are behind the active area of the fan. The inner volume of the heat sink is separated by a plastic tube and is used as a housing for the control board PCB, as shown in Figure 4. The main air flow streams directly through the heat sink fins, where the majority of the power losses have to be dissipated. A bypass air flow, shown with thinner red arrows in Figure 5, can additionally be used to cool the surfaces of the half bridge PCBs and the inner volume with the control electronics without additional cooling effort.

Another important evaluation step of the cooling is the thermal impedance between the SiC MOSFET and the heat sink. For the evaluation, the power device was embedded inside a PCB and mounted with a fixture on the heat sink. The temperature difference between the junction and the heat sink was measured during the cooling phase after the thermal steady condition was reached at known power losses, which was induced with a defined load current. The junction temperature was estimated by means of temperature sensitive voltage drop of the body diode at a constant measurement current and a known calibration function. The thermocouple for the heat sink temperature measurement was located 2

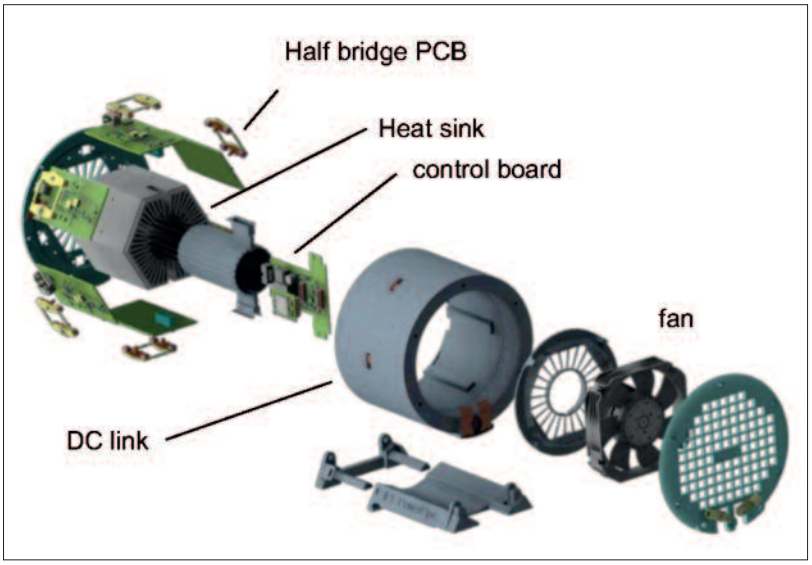

Figure 4: **Exploded view of the prototype inverter**

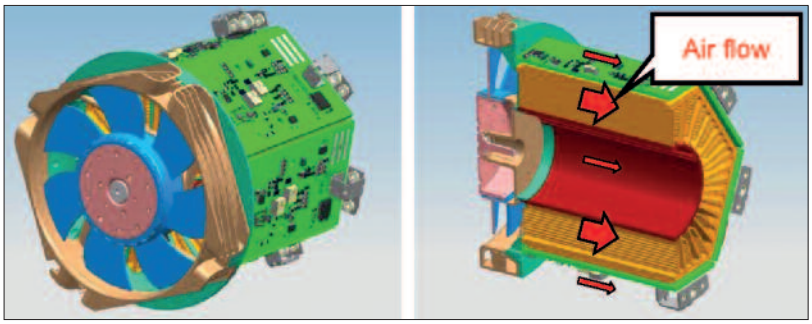

Figure 5: **Inverter cooling**

mm below the heat sink surface in the center of the chip.

DC link and overall inverter assembly

With the higher switching frequency of the SiC inverter, the DC link could be significantly reduced compared to Si-based devices. However, for industrial applications, there is a special demand for DC link capacitance. The inverter has to compensate short blackouts of power grids without failure. Therefore, the capacitance of the DC link is predominantly defined by the rated output power of the inverter. For the designed prototype, the addressed DC/AC output power of 2x27 kW at a rated DC voltage of 600 V requires 1,9 mF DC link capacitance.

The DC link is a series connection of two identical capacitors. With this configuration DCP, DCM and DCN potentials are provided for the three level topology shown in Figure 2. In the proposed inverter design the DC link is a ring-shaped assembly and is located around the hexagonal heat sink. The low profile design of the half bridge PCBs enables a very short and low inductive connection to the DC link capacitors. With this configuration, the whole DC link of the inverter is integrated into the housing. A further advantage is the thermal decoupling of the capacitor from the heat sink and the PCBs. The ring shaped capacitor can be realized by a simple winding process and is already established for automotive applications.

Conclusions

The proposed inverter design and the latest generation of 1200V SiC-MOSFETs lead to a very compact air cooled inverter for industrial applications. Additionally, an improved performance regarding the switching frequency was shown. Crucial for fast switching SiC devices is the low inductive design of the switching cell. The used embedding technology of the power devices into the PCB shows a possible solution to enable higher function integration combined with a low inductive design. The optimized cooling design keeps the PCB temperature relatively low - in an acceptable range for standard lead-free soldering capable FR4 materials and other used devices, placed on the PCB near to the power devices. With the DC link design inside the housing, a space-saving solution with high capacitance, suitable for industrial applications can be realized.

Literature

*A. Hensler, "Air Cooled SiC Three Level Inverter with High Power Density for Industrial Applications", PCIM Europe 2017 Proceedings, pages 2 04 – 21*1