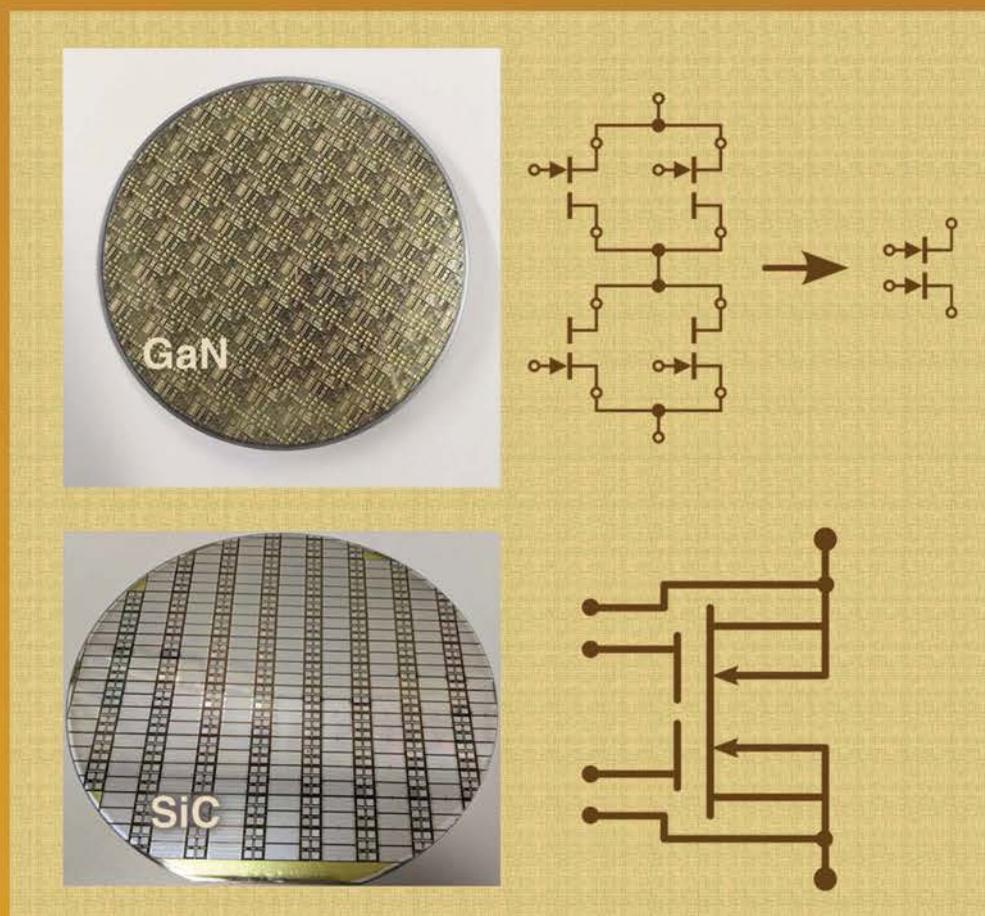


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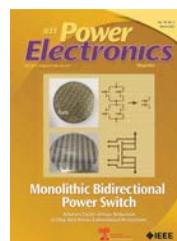


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Monolithic Bidirectional Power Switch

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Current Range	0-1.5 Adc to 0-250 Adc	0-0.2 Adc to 0-600 Adc	0-1.2 Adc to 0-8,000 Adc	0-24 Adc to 0-24,000 Adc



Emerging Monolithic Bidirectional Switches Bring New Energy to WBG Devices

In last ten years or so, wide band-gap (WBG) devices, such as silicon carbide (SiC) and gallium nitride (GaN) power transistors, have made significant progress in reliability, performance, and cost, driving adoption of these devices in a wide range of applications. As a result, the GaN market is projected to be worth about US\$2 billion in revenues by 2027, according to market research firm Yole Développement. In 2021, the GaN market was valued at US\$126 million by Yole. Likewise, Yole expects SiC device market to grow beyond US\$6 billion by 2027 at a CAGR of 34%.

Concurrently, the emergence of monolithic bidirectional switches (MBDS) is expected to open many more opportunities for WBG devices and give this market a new drive that is very much needed. Some mass volume power applications ready to benefit from the control of bidirectional power include electric vehicles (EVs) with interfaces to grid, home, and other vehicles. In addition, distributed and grid-tie power systems using regenerated energy and/or energy storage components, and solid-state circuit breakers are other applications looking for MBDS technology. By enabling these and many other applications with their compelling advantages of high efficiency,

high blocking voltage capability, and low system weight and volume, MBDS will give SiC and GaN technology a shot in the arm.

Three cover features shed light on device development and applications. The first cover feature “The BiDFET Device and its Impact on Power Converters” by B. Jayant Baliga, Douglas Hopkins, Subhashish Bhattacharya, Aditi Agarwal, Tzu-Hsuan Cheng, Ramandeep Narwal, Ajit Kanale, Suyash Shah, and Kijeong Han, presents improvements in Gen-2 SiC bidirectional FET (BiDFET) device with a new chip design and process technology. By comparison, the authors show that the Gen-2 BiDFET device offers low on-resistance with a remarkable 2X reduction in SiC chip area, enabling reduction in chip cost and package size. By successfully validating the operation of the BiDFET die and package, the article highlights the enormous potential of BiDFET for achieving efficient, power-dense, and reliable matrix converters, integrated motor drives, and many other power conversion systems.

The next feature “Monolithic Bidirectional Power Transistors: Opening New Horizons in Power Electronics” by Jonas Huber, and Johann W. Kolar identifies converter families that will benefit from MBDS while briefly discussing most recent MBDS device concepts. Besides driving existing topologies, it will also inspire the derivation of new topologies.

The third feature “Power Conversion Systems Enabled by SiC BiDFET Device” by Subhashish Bhattacharya, B. Jayant Baliga, Douglas Hopkins, Ramandeep Narwal, Aditi Agarwal, Tzu-Hsuan Cheng, Suyash Shah, Ajit Kanale, and Kijeong Han demonstrates the feasibility of matrix converter topologies using monolithic BiDFET, while eliminating the bulky and unreliable dc link capacitors or inductors required for conventional voltage-source or current-source converters in ac-ac and ac-dc applications. The article indicates that the 1.2 kV BiDFET has the potential to disrupt all the applications utilizing 1.2 kV switches, including EV drivetrain, bidirectional EV chargers, industrial motor drives, solid-state transformers, datacenter power supplies, elevator drives, dc microgrids, energy storage grid integration, solid-state circuit breakers, and more.

The next two features are part of the FEPPCON XI Part II sessions. While the article by Pat Wheeler is a road-mapping exercise that discusses how a particular group of power electronics engineers view their respective topics, and gives a list of topics which the attendees of the road-mapping session believed were not covered by any of the PELS TCs, the feature “Reliability of Power Electronic Systems” by Huai Wang, Michael Pecht, Axel Mertens, Rik De Doncker, and Frede Blaabjerg



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provides challenges and opportunities in power electronics reliability. Plus, it discusses how the physics of failure and AI concepts can be used for qualifying electronics reliability and safety.

Likewise, the sixth feature “Selecting the Best Magnetic Core Geometry” by Ira J. Pitel gives some good tips in selecting an optimal core for high frequency transformers and inductors used in power supplies. Finally, in the last feature “Machine-Learning-Based Condition Monitoring of Power Electronics Modules in Modern Electric Drives” by Dinan Li, Panagiotis Kakosimos, and Luca Peretti, the authors demonstrate a data-driven thermal model that utilizes information already residing in most modern electric drives and predicts the case temperature of a power electronics module.

Changing of the Guard, Columns, and News

Starting 1 January, IEEE PELS has a new president. Outgoing president Prof. Liuchen Chang (2021–



FIG 1 Past President Prof. Liuchen Chang (left) passes on the baton to the new President Prof. Brad Lehman (right).

2022) passes on the baton to the new president Prof. Brad Lehman (2023–2024) as depicted in Figure 1. In his first President’s Message, Lehman presents his futuristic vision and programs.

Likewise, in the PSMA Corner, Renee Yawger discusses the involvement of individual committees of PSMA with the regulatory agencies like the U.S. DoE to advance interests of member companies and encourage

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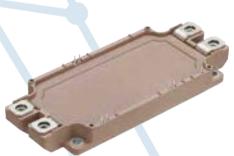
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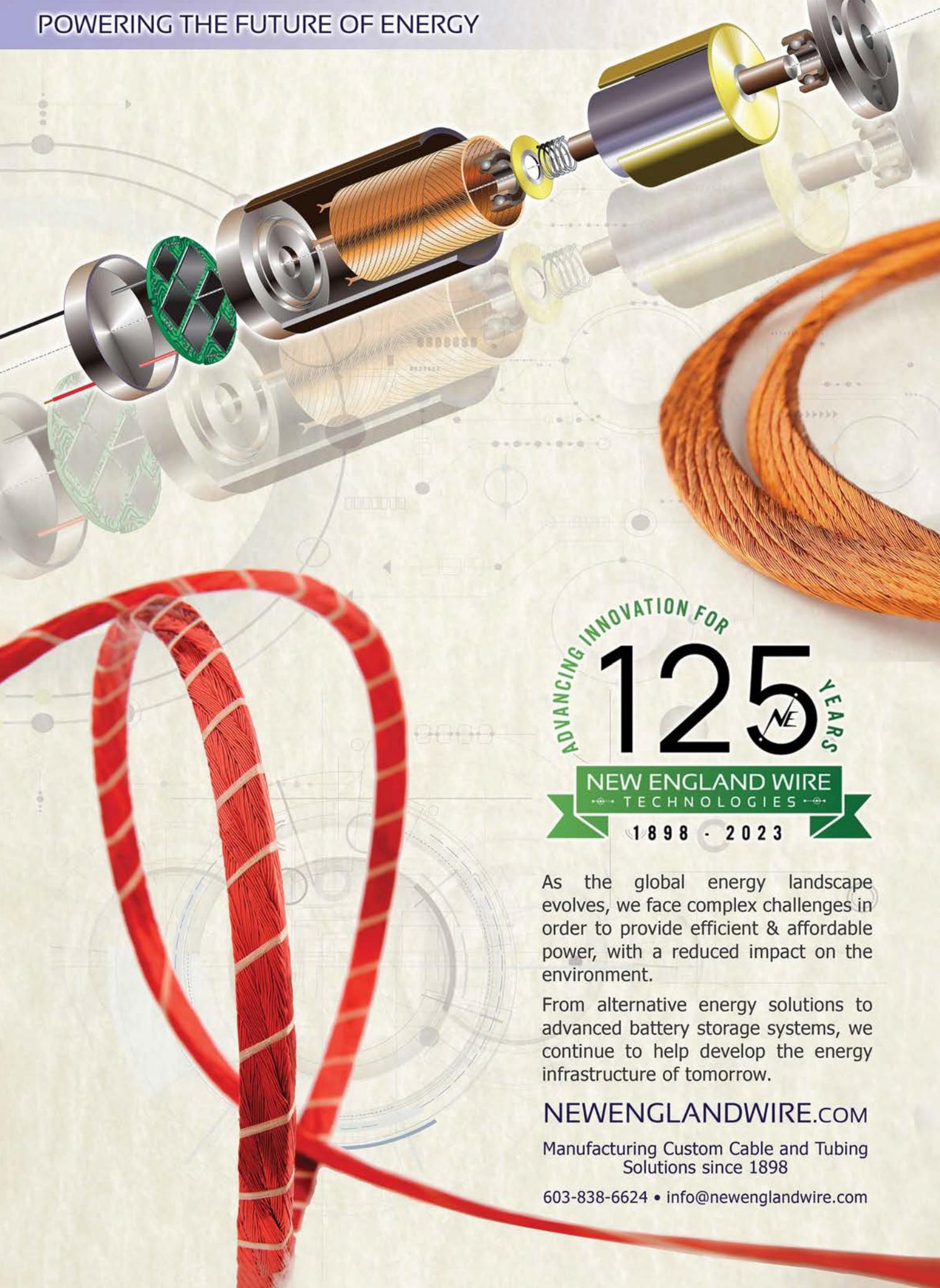




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innovation. While Kristen Parrish uncovers ten years of work done by Women in Engineering (WIE) Committee on its 10th anniversary in the column WIE. And Expert View, written by Victor Veliadis, highlights the development of MBDS and its impact on power electronics technology. He envisions numerous emerging mass volume applications benefitting from MBDS technology.

Similarly, the "Patent Reviews" column, written by Trishan Egram, gives an aerial view of the patent law, and attempts to simplify the understanding of different types of patents. The Industry Pulse, also written by Kristen Parrish, explores blockchain technology and its relationship with cryptocurrencies and what all this means for power electronics. There is no White Hot column in this issue as

Bob White is busy with his company projects. However, he will be back next issue.

The "Students and Young Professionals Rendezvous" column, written by Haifah Sambo, Anshuman Sharma, Nayara Brandão de Freitas, and Joseph P. Kozak, aims to support the professional development of students and recent graduates, further the mission of IEEE PELS and increase the diversity of its membership and volunteering bodies.

As usual, the Society News brings activities from PELS chapters and student branches around the world, and announces a workshop on power electronics in robotics. Finally, the "Event Calendar" provides a year's listing of conferences and workshops.

Thank you for your support throughout the year. As a result, the print and digital versions of the magazine are healthy and delivered on time to our readers. *IEEE Power Electronics Magazine* is committed to bringing timely articles, columns and news items of interest and value to practicing power electronics engineers worldwide. To serve you better and keep this magazine a valuable resource for working power electronics engineers around the world, we look forward to your feedback and suggestions. Now we have a website (<https://pelsmagazine.ieee.org/>) which offers more than what is in the print, and where you can easily provide your feedback. Stay safe and healthy!



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New President: Marching on With Futuristic Vision and Programs

I am humbled by the trust that the IEEE Power Electronics Society (PELS) has placed in me as their elected president of PELS for the next two years (2023–2024). I would especially like to thank the outgoing president, Liuchen Chang, the IEEE PELS staff, and all the volunteers in our society. As we all know, the past few years have been challenging, to say the least, with the ongoing COVID-19 pandemic. Despite these challenges, our outgoing president, executive leaders, and staff have done an incredible job of keeping our society financially strong and as active as ever. Their careful stewardship of our society will allow many new programs to be established in the next two years, with a major reinvestment back into PELS membership.

The field of power electronics is experiencing tremendous growth and advancements, and it is exciting for PELS to be a part of this journey. From renewable energy sources to electric vehicles and beyond, the applications of power electronics are endless. This past year saw our conference portfolio emerge from COVID-19 [e.g., IEEE Applied Power Electronics Conference and Exposition (APEC) and IEEE Energy Conversion Congress and Exposition (ECCE)] and return

to in-person events. With IEEE APEC 2023 in Orlando, FL, USA (19–23 March) and IEEE ECCE 2023 North America in Nashville, TN, USA (29 Oct.–2 Nov.), members will have the opportunity to attend the premier power electronics conferences in two of the most exciting locations in the USA. Hopefully, attendance will be fully back to normal. It should be noted that despite the lower in-person attendance at PELS conferences, because of virtual conference technologies, for the past two years (during COVID-19) PELS conferences remain self-supportive financially.

Concurrently, the journal publications in PELS never saw a drop in number of paper submissions. In fact, page counts increased 5%–10% annually during COVID-19. Our flagship journal, the IEEE TRANSACTIONS ON POWER ELECTRONICS, remains the most downloaded IEEE TRANSACTIONS, which is a clear indication of the immense popularity of power electronics, even across other societies. The products portfolio team even launched the new IEEE PELS-Tube (www.ieeepelestube.org) video channel, which publishes fully reviewed power electronics related videos. It is becoming a source where our members can find high quality instructional material without sifting through the unknown quality of videos on YouTube or other channels. In fact, the digital

and educational growth of activities in IEEE PELS during COVID-19 has become so strong that it led to PELS reorganizing its executive committees to now include IEEE PELS VP for Education starting 2023. We are embracing post-COVID video teaching and adapting our PELS educational programs to modern times.

Are you an IEEE member looking to connect with other professionals in your field and advance your knowledge and skills? Consider joining one of our technical committees (TCs)! With over 3000 people already signed up as TC members, you'll have plenty of opportunities to socialize and collaborate with like-minded individuals. Plus, as a member benefit, participating in a technical committee can help you grow professionally and stay up-to-date in your specific area of expertise. Being able to participate in one of PELS technical committees is one of our great PELS member benefits. Take a look at the various topics of our TCs on our website www.ieee-pels.org, and consider joining a TC today.

Opportunities and Challenges in the Next Two Years

Because of its adaptability and financial care in the past few years, IEEE PELS is ready to emerge in a post-COVID era in a strong position to make major investments in its membership growth and services. We can reinvest our funds into our



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membership and professional growth development, even in riskier yet higher impact endeavors, such as: 1) assisting policy decisions by collaborating with international organizations; 2) expanding local activities with student chapters in countries with burgeoning renewable energy growth (Brazil, India, and others); and 3) developing worldwide collaboration with members (power electronics “hackathons,” industry e-Mentoring, and technology roadmaps). Some strategies we hope to implement in the upcoming years include:

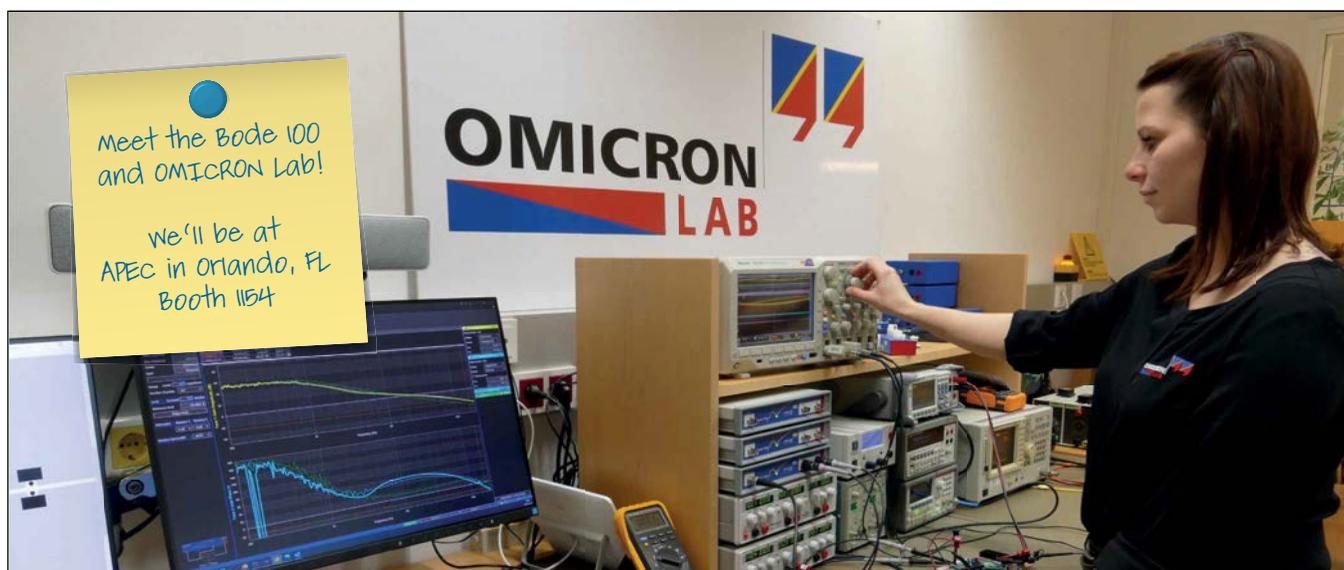
Membership Growth and Development—PELS hopes to: 1) expand Women in Engineering (WIE) and Young Professional (YP) events at almost all PELS sponsored conferences; 2) provide membership subsidies and rewards for our volun-

teers in PELS, particularly for members in developing countries; 3) expand professional development for industry members and entrepreneurs; 4) reinvest PELS resources to maintain a focus on professional development and social network, especially at a local chapter level (Yes, being a member of PELS can also be fun.); and 5) increase membership from ~12k members in 2022 to 15k members by 2025!

Diversity, Outreach, and Training—1) Leverage financial resources to increase WIE events and diversity awareness; 2) grow Ph.D. schools worldwide, which are short-courses delivered by distinguished PELS researchers and lecturers in different countries, focusing on in-person graduate student participation; 3) create public

outreach programs run by PELS members that may have high impact on young elementary and high school students to enter the field of power electronics and renewable energy; and 4) complete the launching of “PELS-Tube” the new educational power electronics video channel with only the best and fully reviewed power electronics related videos.

Maintaining Excellence in Conferences and Products—The financial revenue backbone of PELS are its publications and conferences. We will do our best to expand staff support to assist in running conferences to ease volunteer burden. Further, member communication can be improved through web pages, social media resources, etc. (Any social media savvy PELS members who



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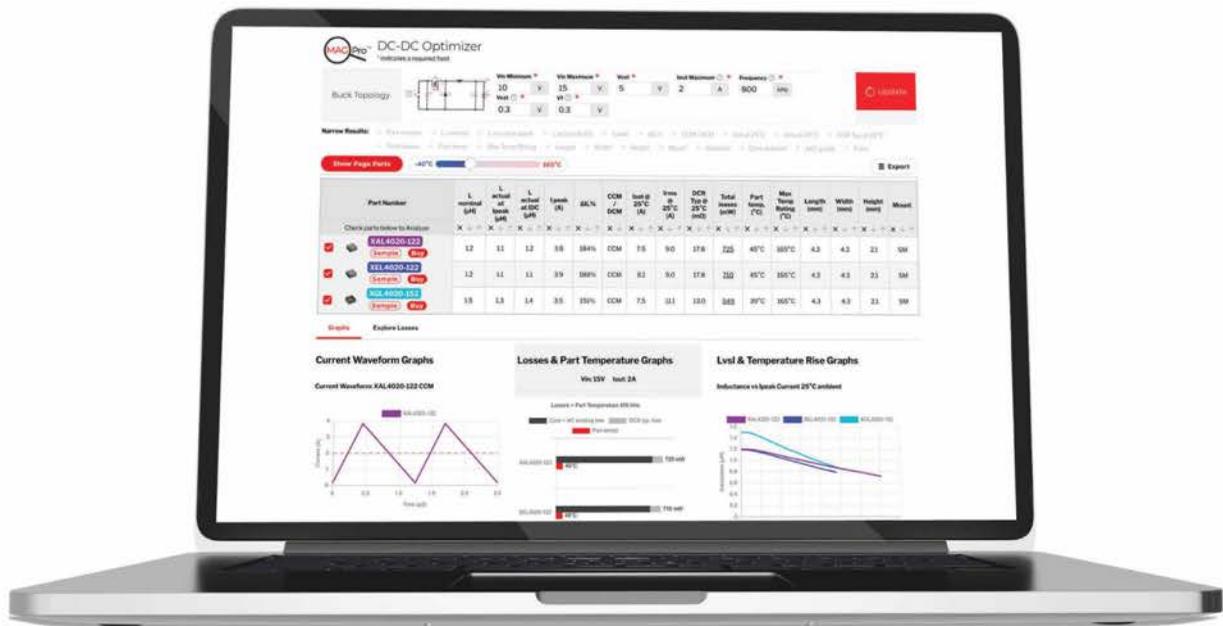
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want to volunteer?) Reviewers and authors might even be rewarded with additional member benefits, which would bring enhanced value to becoming a PELS member.

These are bold programs that will need as many PELS members as possible to volunteer (email me at Brad.pels@ieee.org if you want to help). I am excited for the opportunities and challenges that lie ahead. It is my pledge to serve you (PELS members) with all my effort and dedication as the next president of the IEEE Power Electronics Society!

About the Author

Brad Lehman (lehman@ece.neu.edu) (Fellow, IEEE) has been the IEEE PELS VP of Products since 2019. He was previously the Editor-in-Chief (EiC) of the IEEE TRANSACTIONS ON POWER ELECTRONICS (TPEL) from 2013 to 2018. In his tenure as EiC, TPEL became the most downloaded

IEEE TRANSACTION, as well as providing among the highest net revenue compared to any other IEEE publications. As VP of Products, he helped to initiate the new IEEE OPEN JOURNAL OF POWER ELECTRONICS, the new PELS Education Award, and the educational initiative "PELS-Tube." He has also been an active leader in many other IEEE PELS activities, including a co-founding member of TC-6; conference leadership in ECCE and COMPEL; and chairing the IEEE P1789 standard. He is currently a Professor at Northeastern University (NU), Boston, MA, USA. His research interests include power electronics, with emphasis on the modeling, design, and control of high-density converters. For many years, he has been a dedicated leader in engineering diversity. At NU, he co-founded and directs the "S-POWER" educational and mentoring program. In the past six years, S-POWER has provided scholarships

to more than 160 under-represented minority and women students interested in clean energy fields. He was a recipient of the IEEE PELS 2019 Harry A. Owen, Jr. Distinguished Service Award, the IEEE Modeling and Control Award in 2015, and the IEEE Standards Medallion in 2016. He has been listed in the book *300 Best Professors* (Princeton Review, 2012). Prior to his career as a Professor, he served as the Head Coach for the nationally ranked varsity Georgia Tech swimming and diving team. He claims to have once swum 15 mi in a swimming pool without stopping, although he admits that he may have lost the exact swimming pool lap count (1000 laps). In his spare time, he is an active volunteer in his local community, including regularly leading meal delivery and cooking preparation to homeless shelters around Boston for more than 20 years.



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PSMA Committees Work With Regulatory Agencies to Encourage Innovation

The Power Sources Manufacturers Association (PSMA) (www.pσμα.com) represents more than 100 companies that manufacture power supplies, battery chargers, external power adapters, and the key semiconductors, passive components, and batteries at the heart of all power conversion processes in consumer, automotive, and industrial equipment. It is the responsibility of PSMA to maintain world-class expertise on all aspects of power electronics and to interface on behalf of its members with regulatory agencies to advance the interest of the member organizations. This work falls on the individual committees of PSMA to interface with the regulatory standards and initiatives that will most impact them.

Energy Management Committee and the Department of Energy

PSMA's Energy Management Committee was involved in this type of effort with the U.S. Department of Energy (DoE) in early 2022. The DoE was soliciting public comment on energy conservation standards for external power supplies in Docket Number EERE-2020-BT-STD-006. This is clearly a topic that impacts several member organizations within PSMA, and

the members have a uniquely objective and credible knowledge position on the costs, lead times, and manufacturing challenges associated with meeting tighter energy efficiency requirements. The Energy Management Committee, whose mission is to provide education, support, and recommendations in matters regarding the energy efficiency of power supplies and system power architectures, took the lead on crafting a response reiterating that it is generally beneficial for government agencies to establish stringent but fair levels of energy efficiency standardization. The primary goal of the Energy Management Committee is the establishment of a consistent global standard for energy efficiency.

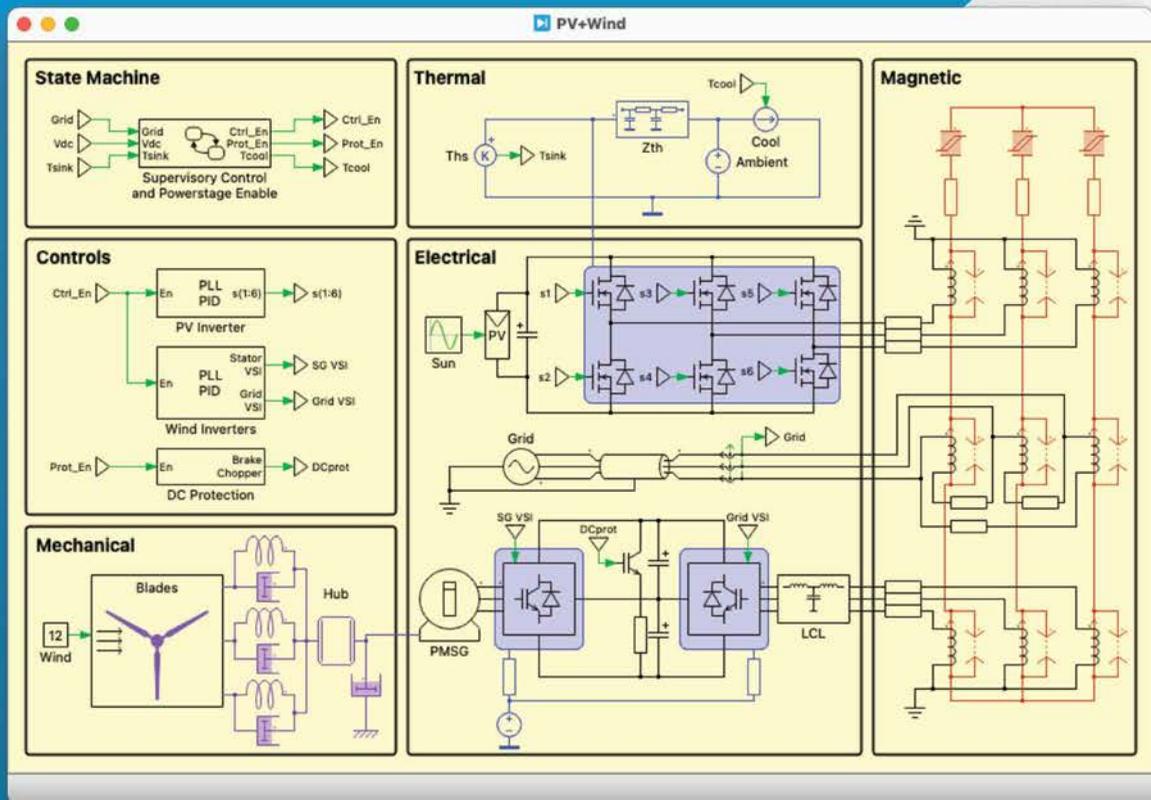
Energy efficiency standards that drive the development of new and better products counteract the forces of commoditization and drive innovation from member companies. Standards, moreover, reduce uncertainty about future market demand for efficient components and encourage long-term investment in emerging technologies such as silicon carbide (SiC) and gallium nitride (GaN) power devices. Further, innovation to meet standards encourages superior circuit design which leverages the talents of engineers in our membership. The goal is to urge the DoE to publish a clear,

long-term roadmap with more aggressive tiers of energy efficiency targets toward which our industry can work over the next 3–5 years.

In the comment letter, the Energy Management Committee encouraged the DoE to update its assumptions because state-of-the-art technologies and products such as GaN-based power supplies can already deliver performance better than those dictated in the proposed standard. The committee encouraged the DoE to raise required efficiency standards given the steady advancements in both power conversion topologies and power device technologies. PSMA strongly supports innovation and clearly defined, aggressive energy efficiency targets provide a roadmap that member companies can use to drive investment and focus on development efforts.

On the DoE's test procedure for external power supplies (Figure 1), the final rule became effective on September 19, 2022. The final rule changes will be mandatory for product testing starting February 15, 2023. Beyond clarifying the scope and better delineating requirements, the test procedure consolidates those requirements to conform to the industry-based Universal Serial Bus (USB) power delivery specifications. On the energy conservation

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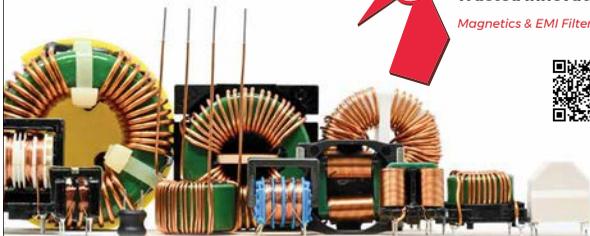
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FIG 1 External power supply. Source: PSMA.

standards for external power Supplies, the DoE is still at the Proposed Rule Stage, having conducted more interviews with manufacturers during the summer as part of the follow up to the DoE's preliminary analysis as published in its Technical Support Document. The next step is the Notice of Proposed Rulemaking or Determination, which is expected in the first quarter of 2023.

Conclusion

PSMA is a non-profit trade association representing more than 100 member companies and has a responsibility to represent its members' interests with the relevant regulatory agencies that have a direct impact on their areas of expertise. This work falls mainly to the individual committees which are always looking for new members to participate.

For a listing of all working committees visit the PSMA website at <https://www.pdma.com/about-psma/organization/working-committees/1>

To become a PSMA member visit <https://www.pdma.com/webforms/pdma-membership-application>

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About the Author

Renee Yawger (renee.yawger@epc-co.com) is the Director of Marketing at Efficient Power Conversion Corporation (EPC) and the Director of Corporate Marketing at EPC Space. She has over 25 years of sales and marketing experience within the semiconductor industry. Prior to joining EPC, she was at Vishay Siliconix for nearly 15 years in various positions in sales support, customer service, and regional marketing. At EPC, she is responsible for the product marketing and marketing communication functions globally. She is also the Vice President of the Board of Directors at PSMA.



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MINI

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AC INPUT: 105 to 125 VAC

OUTPUT VOLTAGE: 3.3 VDC to 48 VDC
OUTPUT CURRENT: 80 mA to 2.5 A



DIN RAIL

to 288 watts
90 to 265 VAC/
110 to 350 VDC

3.3 VDC to 125 VDC
600 mA to 25 A



SWITCHING

to 720 watts
90 to 265 VAC/
110 to 350 VDC
3.3 VDC to 135 VDC
3.3 A to 70 A



LINEAR

to 165 watts
105 to 125 VAC
or 210 to 250 VAC (option)
1.5 VDC to 150 VDC
350 mA to 13.2 A

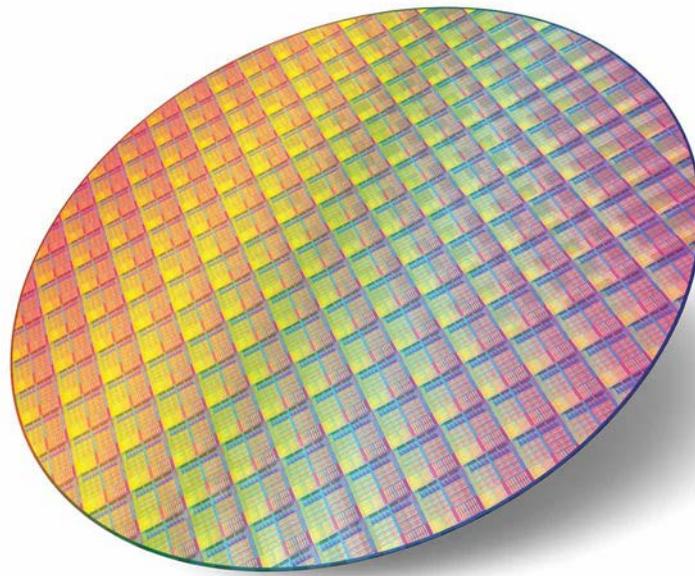


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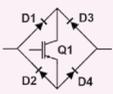
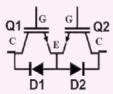
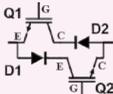
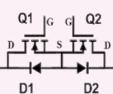
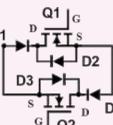
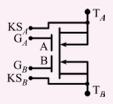
The BiDFET Device and Its Impact on Converters

by B. Jayant Baliga, *Fellow, IEEE*, Douglas Hopkins, Subhashish Bhattacharya, *Fellow, IEEE*, Aditi Agarwal, Tzu-Hsuan Cheng, Ramandeep Narwal, Ajit Kanale, Suyash Sushilkumar Shah, and Kijeong Han

The matrix converter topology for direct ac-to-ac conversion offers elimination of the bulky and unreliable d.c. link capacitors used in the popular voltage-source inverter (VSI) with a front-end rectifier. The resulting more compact and higher efficiency implementation is a desirable solution for a wide variety of applications, such as photovoltaic energy generation, motor drives, and energy storage systems.

The development of matrix converters has been hampered by the lack of availability of commercial bidirectional power switches with the ability to block high voltages in the first and third quadrants, carry on-state current in both quadrants with low voltage drop, exhibit large forward-biased safe-operating-area (FBSOA), and low switching power losses. Consequently, many implementations have been tried in the past using discrete devices, as listed in Table 1. Two implementations utilize commonly available asymmetric blocking IGBTs, while two cases make use of SiC power MOSFETs. They generally have a large parts count (4–6 individual switches) that occupies significant space in the converter where multiple bidirectional switches (BDS) are required. They also have a high on-state voltage drop that degrades efficiency. One implementation utilizes symmetric blocking IGBT to achieve a low parts count (2), but its switching losses are unacceptably high.

Table 1. Comparison of fabricated 1.2 kV BiDFET with previous BDS implementations.

Comparison of fabricated 1.2 kV 20 A BiDFET with previous bidirectional switch implementations				
Switch Configuration	Description	Number of components	On-State Voltage Drop (V)	Switching Loss
	Diode Bridge + Asymmetric IGBT Neft & Schauder, IEEE Trans. Ind. Appl., vol. 28, pp. 546–551, 1992	5	8.6 [2 diodes + 1 IGBT]	High
	Asymmetric IGBTs + Freewheeling diodes Moghe et al., ECCE, pp. 3848–3855, 2012	4	5.8 [1 diode + 1 IGBT]	High
	Back-to-back symmetric IGBTs Takei et al., ISPSD, pp. 413–416, 2001	2	2.2 [1 symmetric + 1 IGBT]	Very High
	SiC Power MOSFETs + JBS diodes Safari et al., IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2584–2596, 2014	4	3.1 [1 diode + 1 MOSFET]	Low
	Back-to-back SiC Power MOSFETs + antiparallel and series JBS diodes Ahmed et al., IEEE Trans. Power Electron., vol. 32, pp. 1232–1244, 2017	6	3.1 [1 diode + 1 MOSFET]	Low
	Four-terminal SiC Monolithic BiDFET	1	1.0 [1 BiDFET]	Low

GEN-1 BiDFET

The silicon carbide (SiC) BiDirectional FET (BiDFET) device was proposed [1] and developed to create a single chip four-terminal bidirectional device with low on-state drop and switching losses for matrix converters. A cross-section of the 4-terminal monolithic SiC BiDFET Gen-1 device is shown in Figure 1. It contains two adjacent 1.2 kV SiC JBSFETs integrated in a single chip. A JBSFET is a MOSFET structure with an integrated JBS diode to suppress conduction of the body diode in the third quadrant. The drain terminals of JBSFET-1 and JBSFET-2 are internally connected via the common N⁺ substrate and back-side metallization. Each JBSFET cell contains a MOSFET portion integrated with a JBS diode. The JBSFETs operate with vertical current flow, like typical high voltage power MOSFETs, ensuring uniform current distribution within the active area. The power MOSFET body diode is deactivated using the integrated JBS diode within each cell to reduce switching losses and avoid the bipolar degradation phenomenon [2]. The two

These results demonstrate that the BiDFET devices can be paralleled to increase the power handling capability.

JBSFETs provide high voltage blocking capability, low on-state resistance, excellent FBSOA, and fast switching performance in each quadrant. High voltage blocking capability is achieved in both quadrants when the gates G1 and G2 are shorted to the respective terminals T1 and T2. On-state current flow occurs in both quadrants with low on-state resistance when a gate bias (typically 20 V) is applied to both gates G1 and G2 with respect to terminals T1 and T2. Power switching is performed in the first quadrant by toggling gate bias G1 applied to JBSFET1 with gate G2 held at the on-state gate bias. In the same manner, power switching is performed in the third quadrant by toggling gate bias G2 applied to JBSFET2 with gate G1 held at the on-state gate bias.

The first generation (Gen-1) BiDFET device was designed using the JBSFET cell cross-section shown in Figure 2(a). It has a half-cell width of 6.1 μm to accommodate the JBS diode within the MOSFET cell. The accumulation-mode channel was chosen to obtain a mobility of 20 cm²/V-s with a channel length of 0.5 μm to minimize the channel

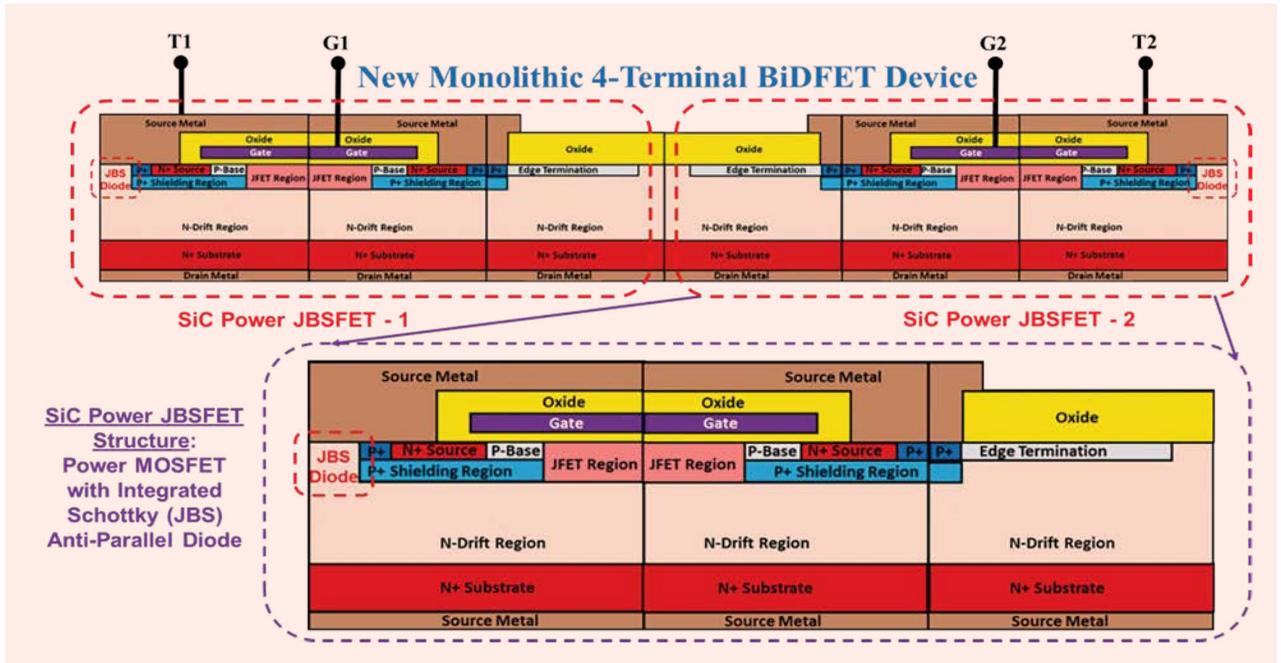


FIG 1 The BiDFET device—Gen 1 implementation.

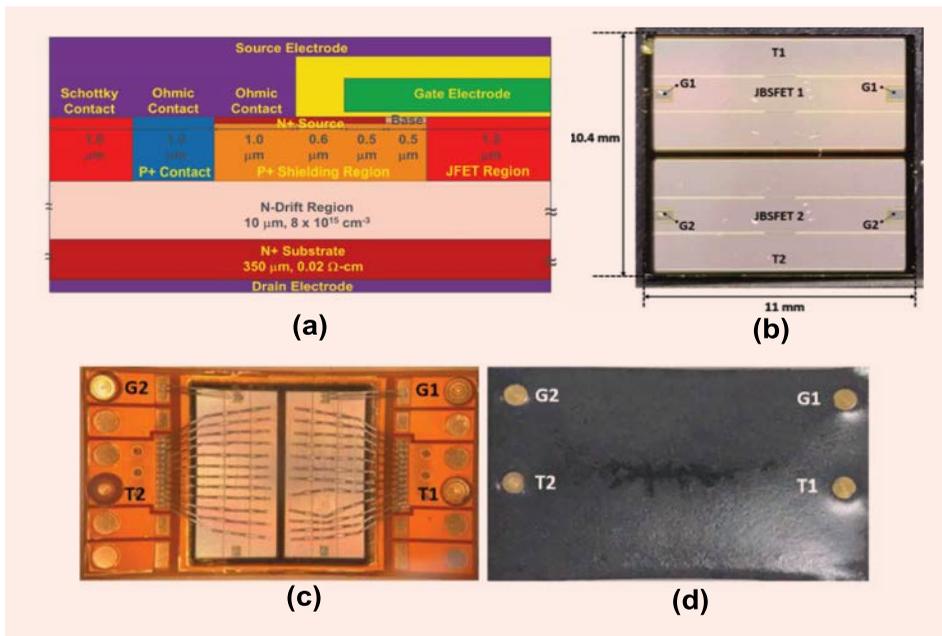


FIG 2 Gen-1 BiDFET device implementation: (a) JBSFET cross-section; (b) BiDFET chip image; (c) custom designed 4-terminal package; (d) encapsulated module.

resistance contribution. The devices were fabricated on n-type epitaxial layers with doping concentration of $8 \times 10^{15} \text{ cm}^{-3}$ and $10 \mu\text{m}$ thickness to achieve a blocking voltage above 1400 V using the hybrid-JTE edge termination [8]. An image of the Gen-1 BiDFET chip is shown in Figure 2(b) with JBSFET1 at the top and JBSFET2 at the bottom. The chip layout contains gate bus bars to distribute the drive voltage with two gate pads per JBSFET for convenient packaging. Since the JBSFET cells have a specific on-resistance

of $11.25 \text{ m}\Omega\text{-cm}^2$, an active area of 0.45 cm^2 was chosen to achieve a total on-resistance of $50 \text{ m}\Omega$ for the BiDFET. The Gen-1 BiDFET die size is $1.04 \text{ cm} \times 1.10 \text{ cm}$. The devices were fabricated using the NCSU PRESiCe process technology at a commercial foundry X-Fab, TX [9]. The BiDFET process technology is similar to that used for manufacturing SiC power MOSFETs and JBS diodes making these devices commercially viable. After wafer level characterization, the Gen-1 BiDFET dies were mounted in a custom-designed module, as shown in Figure 2(c), with sufficient wire bonds in the active area to reduce the package resistance

to less than $1 \text{ m}\Omega$. Figure 2(d) shows the encapsulated 4-terminal module.

The measured blocking characteristics for the Gen-1 BiDFET device at $25 \text{ }^\circ\text{C}$ are shown in Figure 3(a) [3]. The device can support over 1.4 kV in both the first and third quadrants when the gates G1 and G2 are shorted to the respective terminals T1 and T2 as shown in the inset with the device symbol. JBSFET1 supports the voltage in the first quadrant, while JBSFET2 supports the voltage in the

third quadrant. The device exhibits the desired gate voltage controlled output characteristics with saturated drain current at lower gate bias voltages (e.g., 5 V) as shown in Figure 3(b) at 25 °C. The Gen-1 BiDFET has a total on-resistance of 50 mΩ at a gate bias of 20 V at 25 °C. The device can handle 20 A at a drain bias of 1 V consistent with Table 1. The integrated JBS diodes have a voltage drop of less than 2.5 V to ensure effective bypassing of the MOSFET body diode [2]. The turn-on, turn-off, and total switching losses obtained using double pulse testing of the BiDFET devices [4], performed at a drain supply voltage of 800 V and current of 10 A, were 620, 300, and 920 μJ. The total switching loss was observed to decrease with increasing temperature to 140 °C.

The BiDFET devices can be paralleled to increase the current handling capability for use in higher power converters. This was demonstrated by building a half-bridge module containing two paralleled BiDFET devices in the upper and lower leg, as shown in Figure 4(a). The encapsulated module is shown in Figure 4(b). The measured blocking characteristics for the Gen-1 paralleled BiDFET devices are shown in Figure 5(a) in both quadrants. The device can support over 1.4 kV in both the first and third quadrants when the gates G1 and G2 are shorted to the respective terminals T1 and T2. The device exhibits the desired gate voltage controlled output characteristics, as shown in Figure 5(b). It has a total on-resistance of 25 mΩ at a gate bias of 20 V, which is half that of the single Gen-1 BiDFET chip as expected. Double pulse testing of the paralleled BiDFET devices was performed at a drain supply voltage of 800 V and current of 20 A. The extracted turn-on, turn-off, and total switching losses were 1350, 460, and 1810 μJ, which are about twice that of the single Gen-1 BiDFET chip as expected. These results demonstrate that the BiDFET devices can be paralleled to increase the power handling capability.

GEN-2 BiDFET

A significant enhancement in the BiDFET die performance has been recently achieved with an innovative new chip design and process technology. The integration of the JBS diode inside the MOSFET cell for the Gen-1 chip design produces a large cell pitch of 6.1 μm with low channel density. In order to

simultaneously obtain ohmic contacts to the N⁺ and P⁺ regions for the MOSFET while achieving a low leakage current Schottky contact to the drift region for the JBS diode, it is necessary to anneal the Nickel contacts at 900 °C [2]. This process produces an N⁺ source contact specific resistance of 0.8 mΩ-cm². Modelling of the JBSFET on-resistances has shown that the total on-resistance is significantly increased due to the large cell pitch and high source contact resistance [5].

A much lower specific on-resistance for the MOSFET cells within the Gen-2 BiDFET device was achieved by separating the JBS diodes from the MOSFET cells and locating them at four corners of the chip. The MOSFET cell size could then be reduced to 2.8 μm, as shown in Figure 6(a) right side, to achieve 2.2x increase in channel density. The contact to the P⁺ region is made orthogonal to the cross-section to make the cell pitch smaller. The Nickel contact to the N⁺ source region of the MOSFET was annealed at 1000 °C to reduce the specific contact resistance to 0.05 mΩ-cm². The specific on-resistance of the fabricated MOSFET cell with this design and process was measured to be 4.5 mΩ-cm², an improvement by a factor of 2.5-times compared with the Gen-1 devices. In order to ensure effective bypassing of the MOSFET body-diode, 10% of the active area was ascribed to the JBS diodes while keeping the die footprint the same as that of the Gen-1 devices. The Titanium contact to the JBS diodes was separately fabricated to achieve the Schottky

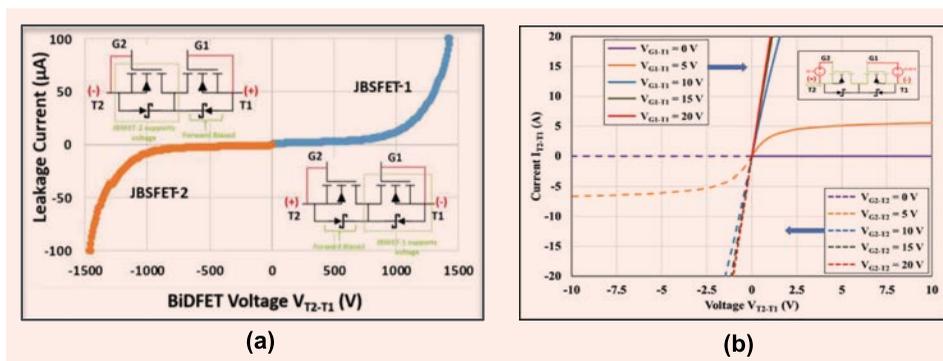


FIG 3 Gen-1 BiDFET device: (a) blocking characteristics; (b) output characteristics.

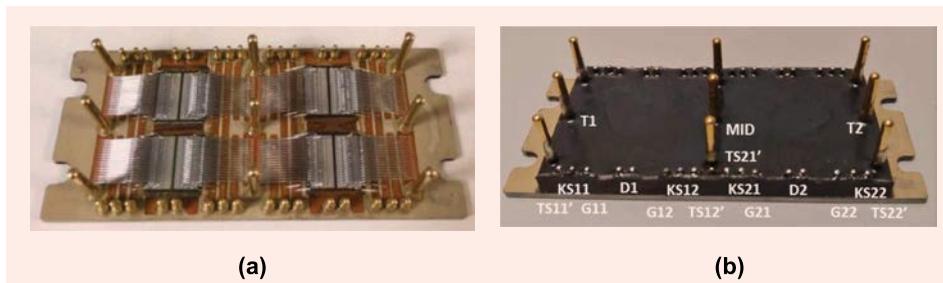


FIG 4 Gen-1 BiDFET paralleled device implementation: (a) internal construction; (b) encapsulated module.

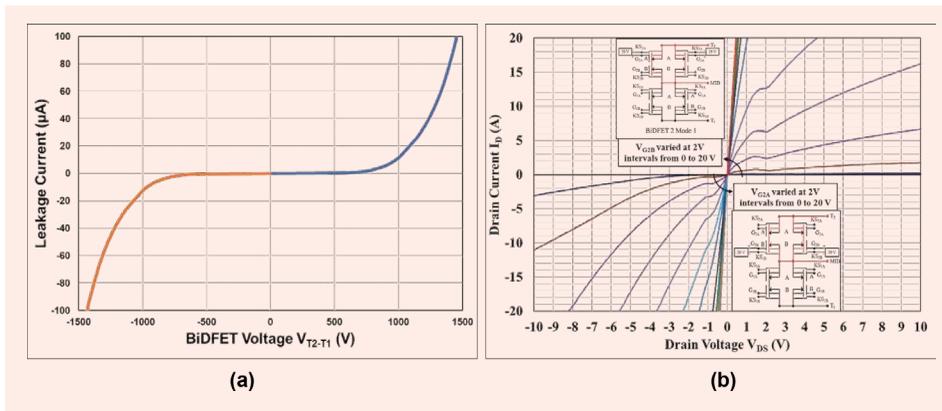


FIG 5 Gen-1 BiDFET paralleled devices: (a) blocking characteristics; (b) output characteristics.

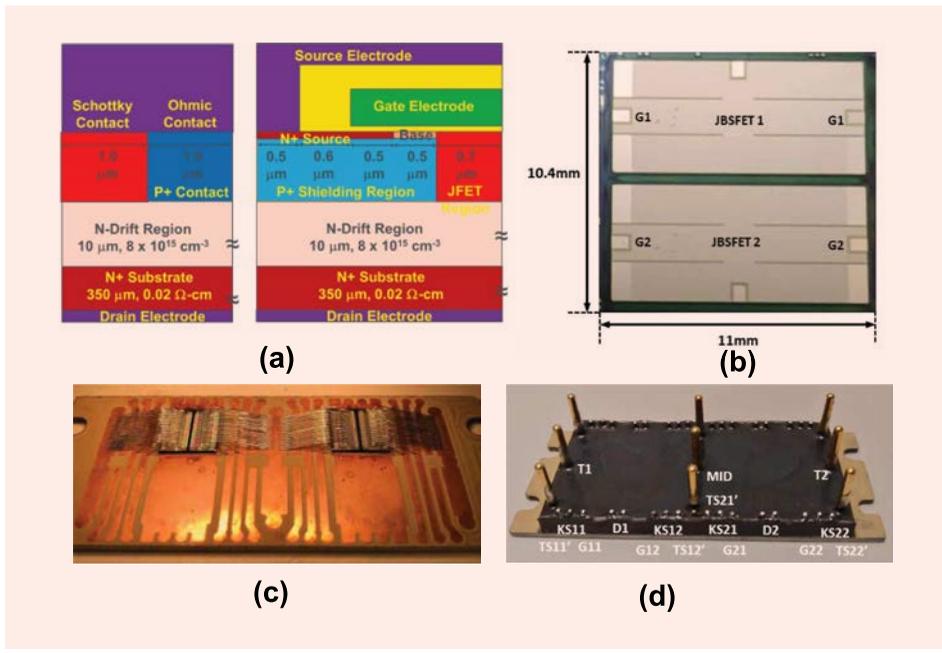


FIG 6 Gen-2 BiDFET device implementation: (a) JBS diode and MOSFET cross-sections; (b) BiDFET chip image; (c) custom designed 4-terminal package; (d) encapsulated module.

contact. JBS diode test elements with an active area of 0.045 cm^2 (the same value as the JBS diodes inside the JBSFETs in the Gen-2 chip) fabricated with the Gen-2 BiDFETs were found to have an on-state voltage drop of less than 2.5 V confirming effective bypassing of the MOSFET body diodes in the BiDFETs. The MOSFET cells in the remaining 90% of the active area have a calculated on-resistance of $12 \text{ m}\Omega$ for each JBSFET. Consequently, the new chip architecture and process creates a Gen-2 BiDFET device with an on-resistance of about $25 \text{ m}\Omega$, which is half that of the Gen-1 device, *while maintaining the same chip size*. This is a major technological improvement for SiC BiDFETs in terms of reducing the die cost and module size in half. An image of the Gen-2 BiDFET chip is shown in Figure 6(b). The regions with the JBS diodes in the four corners of the chip are visible

due to a slight difference in the metal texture. The Gen-2 BiDFET chips were packaged in the same half-bridge module designed for the Gen-1 paralleled devices as shown in Figure 6(c) and occupy half the space. The encapsulated module is shown in Figure 6(d).

The measured blocking characteristics for the Gen-2 BiDFET device are shown in Figure 7(a) in both quadrants. The device can support 1.4 kV in both the first and third quadrants when the gates G1 and G2 are shorted to the respective terminals T1 and T2. This Gen-2 BiDFET has sharper breakdown characteristics than the Gen-1 devices. The device exhibits the desired gate voltage controlled output characteristics with saturated drain current at lower gate bias voltages, as shown in Figure 7(b). It has a total on-resistance of $27 \text{ m}\Omega$ at a gate bias of 20 V, which is close to the design value. Double pulse testing of the Gen-2 BiDFET devices was performed at a drain supply voltage of 800 V and current of 20 A. The extracted

turn-on, turn-off, and total switching losses were 1120, 250, and $1370 \mu\text{J}$. These values are smaller than those observed for the paralleled Gen-1 BiDFET devices.

A comparison between the Gen-1 BiDFET technology with the Gen-2 BiDFET technology is provided in Table 2. The improvements in performance are shown in the right-hand column. It can be seen that a BiDFET device on-resistance of $25 \text{ m}\Omega$ has been achieved with a remarkable 2-times reduction in SiC chip area, which is important for the reduction of chip cost and package size. The capacitances for the single Gen-2 BiDFET chip are smaller than those measured for the paralleled Gen-1 BiDFET devices. In particular, the output capacitance (C_{OSS}) for the Gen-2 BiDFET is 1.75 times smaller, which leads to the reduced switching losses measured for the Gen-2 BiDFET devices.

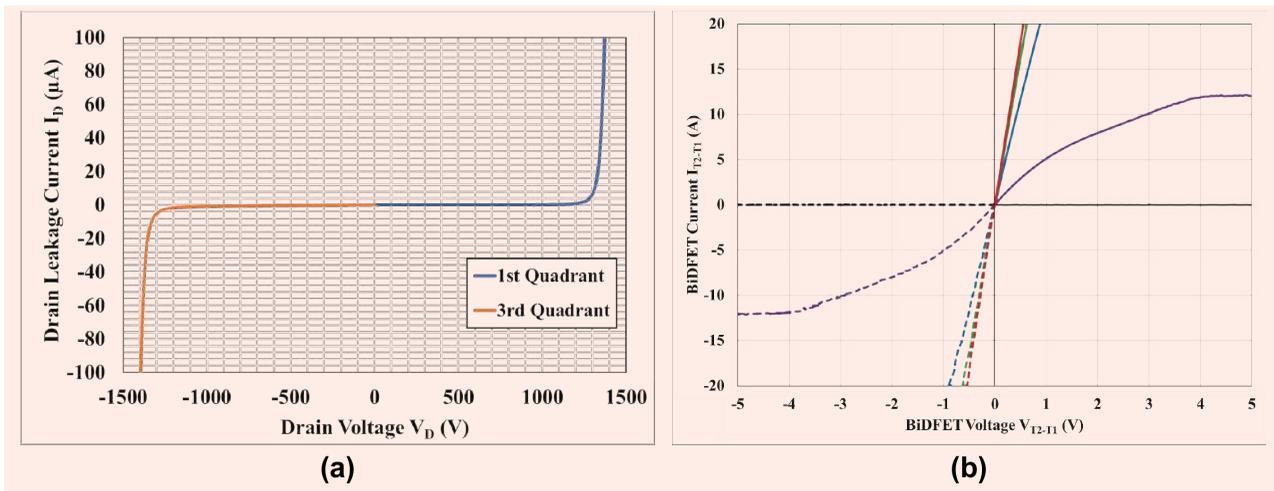


FIG 7 Gen-2 BiDFET device: (a) blocking characteristics; (b) output characteristics.

Table 2. Comparing Gen-1 and Gen-2 BiDFETs.

Parameter, Units	Gen 1 (2 Chips)	Gen 2 (1 Chip)	Improvement
Chip Area, cm ²	2.28	1.14	2x
R _{DS,ON} , mΩ	25	27	-
g _M , S	15	15	-
C _{ISS} , pF	15100	11730	1.3x
C _{OSS} , pF	1050	600	1.75x
C _{RSS} , pF	70	70	-
E _{ON} , μJ	1350	1120	1.2x
E _{OFF} , μJ	460	250	1.8x
E _{TOTAL} , μJ	1810	1370	1.3x

Advanced Packaging Approach

The target for this research was a low cost, reliable converter operating in a harsh environment with preferred convective cooling. Since the BiDFET has very low loss, an advanced alternative packaging approach was adopted. An investigation was undertaken to compare the use of ultra-thin epoxy resin composite dielectric (ERCD) as a replacement to traditional DBC that uses plate ceramic. The ERCD material recently introduced by RISHO KOGYO Co. Ltd. is characterized as having 10 W/mK, 40 kV/mm B.V., modulus of 53 Gpa, operation at ≤300 °C, and thickness of 120 μm. The material is available as a metalized film, laminate or clad on thick copper to create an insulated metal substrate. Use of an organic approach allows for a metalized substrate, or complete module, to be processed by high-end PCB companies at substantially reduced cost and turn-around time.

To compare ceramic to ERCD, a two-sided module structure, Figure 8, was designed and simulated in ANSYS

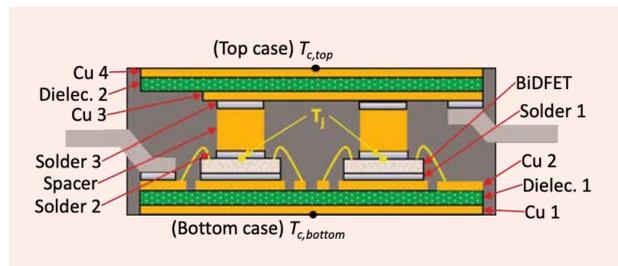


FIG 8 Two-sided power package to compare ceramic and ERCD dielectric isolated substrates.

as reported in [6]. Two SiC die were mounted and encapsulated to allow heat flow from both surfaces. Spacers were assumed to cover 60% of the die area. For a two-sided structure, four possible combinations of topside and bottom-side dielectrics of ceramic and ERCD were considered, with further consideration of two types of ceramic, Al₂O₃ and AlN. The ceramics were 380 μm thick clad with 127 μm of Cu, and ERCD was 120 μm thick with 100 μm Cu. The thermal conductivities were 24, 170, and 10 W/mK for Al₂O₃, AlN and ERCD respectively. Comparative results for thermal resistance are shown in Figure 9 and shows that the ERCD R_{jc,eq} is 10% better than Al₂O₃. Though ERCD has lower conductivity, the thinness allows the conductance to be higher. Since cost is of concern and the power dissipation capability with ERCD is well within the project requirements, the more costly AlN and ceramic processing can be avoided. Since cost is of paramount concern, a 19 mm × 32 mm exemplar substrate was provided to three vendors for pricing. The ERCD approach was one third or less than Al₂O₃ DBC, Figure 10. The ERCD is rated for continuous operation up to 300 °C as noted in the paragraph above. Over temperature of the BiDFET would not noticeably affect the cost comparison, and the reliability issues would be dominated by chip attachment in both DBC and ERCD.

The Gen-I BiDFET unencapsulated single-sided module mounts the die on an ERCD insulated metal substrate (eIMS) as shown in Figure 11(a) [6]. The ANSYS thermal analysis,

Figure 11(b), shows a 101 °C worst case temperature in a 66 °C environment with conductive cooling with $I_D = 20$ A. The Gen-2 has much lower loss, as discussed above, and is well matched to the more cost effective advanced ERCD packaging approach.

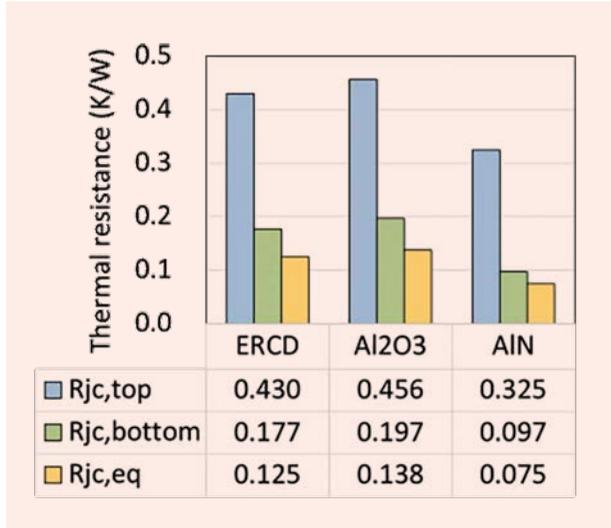


FIG 9 Thermal resistance of the two-sided package comparing ceramic and DBC.

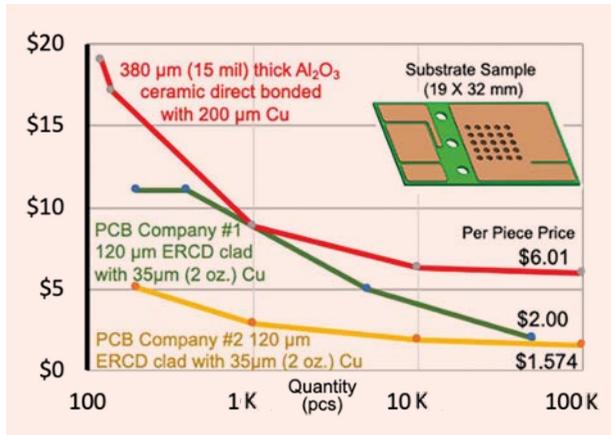


FIG 10 Comparative pricing of advanced ERCD substrate and Al₂O₃ DBC.

Impact on Converters

A four-quadrant switch enables matrix converter topologies that do not require bulky inductors or electrolytic capacitors for their operation. Yet such converters are not popular commercially, primarily due to a greater number of devices than voltage source converters. The impact of BiDFET invention on the commercial viability of such converters can be understood by accounting BiDFET effect on three of the converter performance metrics: reliability, size, and efficiency.

The reliability of the converter depends on the number of components and the reliability of each component. The BiDFET can replace four-quadrant switch implementations utilizing multiple discrete devices, which leads to not only a lower number of devices per converter but also a lower number of unreliable wire bonds. A monolithic device will obviously require lesser space than discrete devices based four-quadrant switch. The switches' reduced size and simpler packaging facilitate a smaller inductance commutation loop and, consequently, lesser over-voltage for the same di/dt transition or faster di/dt transitions for the same overvoltage. The switching loss of devices typically decreases with faster di/dt transitions.

Furthermore, the BiDFET constituent JBSFETs offer numerous advantages over MOSFETs. JBSFET has lower turn-on loss and almost constant total switching loss over the temperature variation because the JBS diode has a much lower reverse recovery charge than MOSFET's P-i-N body diode. The JBS diode also has almost no variation in stored charge or reverse recovery time with variation in dead-time duration, causing a smaller turn-on current spike and hence allowing faster dv/dt transition, which further decreases the device switching loss.

Depending on the converter modulation scheme, one constituent FET of BiDFET might conduct current for a longer duration or switch more often than the other constituent FET. For example, in a single-phase matrix converter, one constituent FET will remain on for the entire positive ac half-cycle while the other is modulated and vice versa during the negative ac half-cycle. The temperature cycling of these constituent FETs in

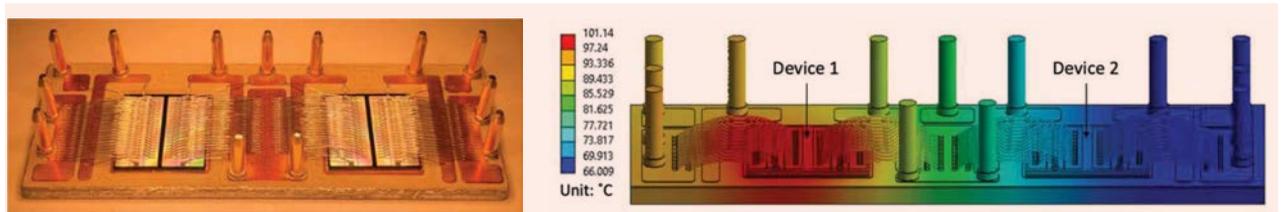


FIG 11 (a) Gen-1 BiDFET mounted on ERCD insulated metal substrate [6]. (b) Temperature distribution for a Gen-1 BiDFET operating with an $I_d = 20$ A.

a BiDFET will be narrower than discrete devices in a four-quadrant switch implementation. Due to the monolithic nature of BiDFET, the losses in one FET will heat up the other FET as well. This narrower temperature cycle of the device will enhance its reliability further. This phenomenon is expected to provide significant benefits in motor drive applications with lower [e.g., < 10 Hz] output frequency.

Therefore, the BiDFET device has enormous potential for efficient, power-dense, and reliable matrix converters that are fundamentally better than voltage source converters in some applications. The performance of current source converter, T-type voltage source converter, Vienna rectifier, hybrid third-harmonic injection based rectifier, auxiliary resonant commutated pole inverter, and other converters utilizing four-quadrant switches, can also be improved through the use of BiDFET device. The operation of BiDFET die and package has been successfully validated through switching tests at 800 V, 20 A [4], and continuous operation of the single-phase isolated ac-dc converter hardware at 2.3 kW, 400 V_{DC} input, and 277 V_{RMS} output [7].

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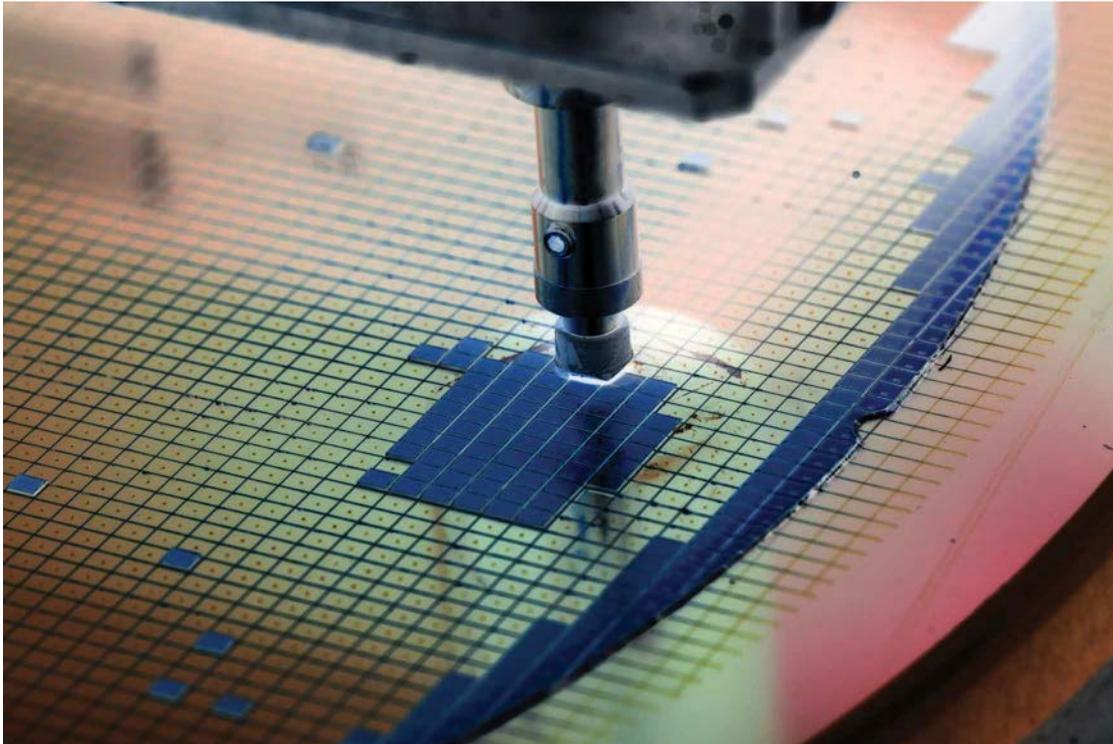
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Monolithic Bidirectional Power Transistors

Opening New Horizons in Power Electronics

by Jonas Huber and Johann W. Kolar

Today's global megatrends—loosely defined as long-term trends that shape societies and economies worldwide—include, e.g., the transition to a fully renewable energy supply and the establishment of evermore stringent efficiency requirements for industry. Similarly, the trend of rapid global urbanization creates a need for sustainable mobility. The digital disruption contributes to increased electricity demand but on the other hand enables solutions such as smart energy networks or design, control, and

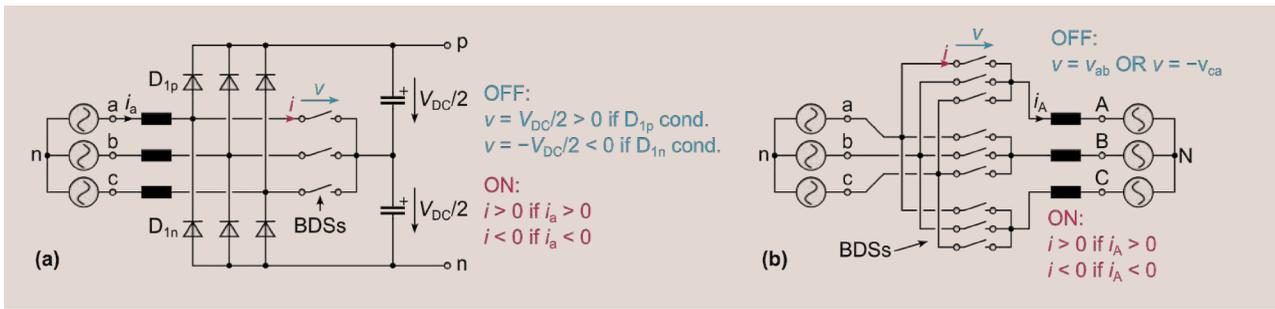


FIG 1 Examples of converter topologies that require switching elements with bipolar voltage blocking and bidirectional current conduction capability, i.e., bidirectional switches (BDSs). (a) Vienna rectifier [1], a widely-used boost-type (note the grid-side boost inductors) topology for power-factor-correcting rectifiers. (b) Direct matrix converter [2], [3], an ac-ac motor drive topology with only nine BDSs.

monitoring systems supported by artificial intelligence (AI). Ultimately, future energy systems should seamlessly integrate, e.g., renewable energy sources, electric mobility, and industrial plants, i.e., they will be mostly electric.

Power electronics is a key enabling technology for this transition to an all-electric society. Power electronic systems are and will be ubiquitous—be it as grid interfaces for datacenter power supplies (datacenters and data transmission networks consumed about 2%–3% of the world’s 2020 electricity production) or ultra-fast electric vehicle (EV) charging stations (the U.S. government targets a 50% EV market share by 2030), or as smart motor drives for industry automation (45% of all electricity powers electric motors, driving a wide variety of loads from pumps to highly dynamic actuators in robotics applications).

Both broad categories of power electronic converters, i.e., grid interfaces and motor drive systems, comprise widely used topologies that require switching elements with the capability of bipolar voltage blocking in the OFF state *and* bidirectional current conduction in the ON state, i.e., bidirectional switches (BDSs). Figure 1 shows two prominent examples: the Vienna rectifier (VR) [1] is a unidirectional three-phase, three-level ac–dc grid interface, widely used in telecom power supplies or EV chargers. The direct matrix converter (DMC) [2], [3] realizes ac–ac conversion for motor drives with only nine BDSs.

However, none of the common power semiconductor devices [Figure 2(a)–(e)] provides the BDS functionality that these two—and many more—converter topologies require. Therefore, today’s implementations must employ

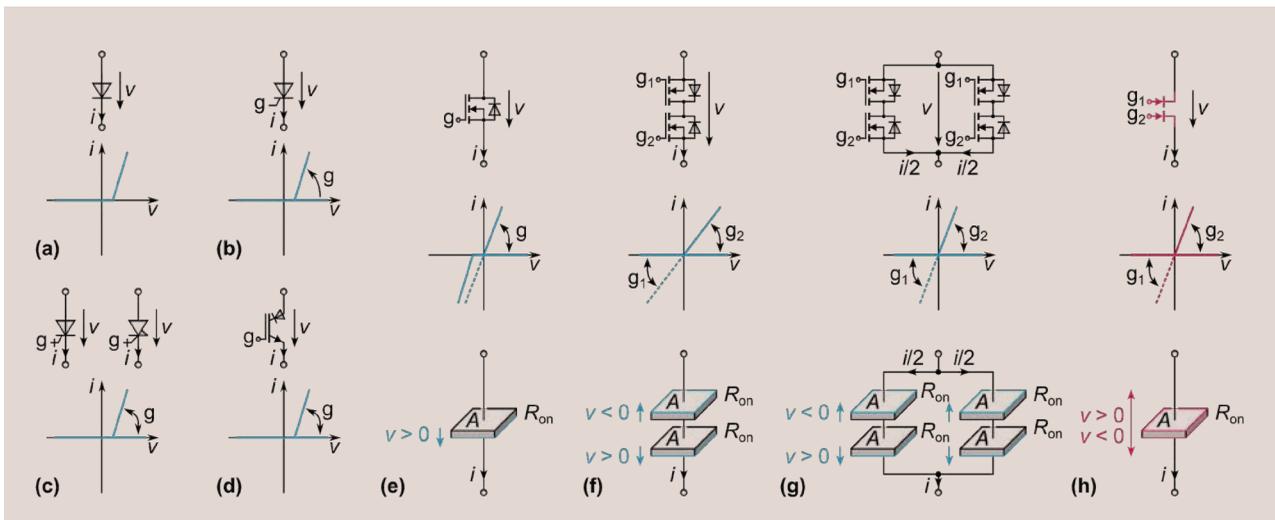


FIG 2 Common power semiconductors and their v - i characteristics. (a) Diode. (b) Thyristors (without turn-off capability), (c) GTOs and IGCTs (with turn-off capability), and (d) RB-IGBTs (with reverse-blocking capability) can support both blocking voltage polarities but conduct only one current direction. (e) MOSFETs, in contrast, can conduct current in both directions but only support one polarity of the blocking voltage. For a given blocking voltage rating and a given chip area A , an on-state resistance of R_{on} results. (f) An inverse-series connection of two MOSFETs realizes BDS functionality but with a total resistance of $2 R_{on}$; (g) paralleling a second such inverse-series arrangement again results in a total resistance of R_{on} but requires a chip area of $4 A$, i.e., four times that of a single transistor. (h) Dual-gate single-drift-region monolithic bidirectional switch (MBDS) with a single drift region used for blocking either voltage polarity, thus providing BDS functionality with a total on-state resistance R_{on} and only a minor increase of the chip area compared to a standard device without reverse-blocking capability.

combinations of existing discrete devices. For example, an inverse-series connection of two MOSFETs achieves BDS functionality [Figure 2(f)], but the total ON-state resistance increases to twice that of a single device. To prevent this, a second such inverse-series arrangement must be connected in parallel [Figure 2(g)]. Thus, realizing BDS functionality with conventional power semiconductors, specifically with MOSFETs, comes at the price of a fourfold increase in chip area usage.

This factor-of-four penalty has, to some extent, hindered the two circuit topologies shown in Figure 1 from exploiting their full potential and might have slowed down the adoption of further topologies discussed throughout the article, which otherwise would offer significant advantages such as direct ac–ac conversion. With *monolithic* bidirectional switches (MBDSs) and, in particular, MBDSs with a single shared drift region for blocking either voltage polarity and two gates (one for controlling each blocking voltage polarity) as shown in Figure 2(h) nearing market entry, a reevaluation of these converter topologies becomes necessary. It is important to highlight that even though the common acronym MBDS only includes the functionality (BDS) and the realization (M) but not the key aspect of having just a single drift region, in the following MBDS refers to dual-gate single-drift-region devices like that shown in Figure 2(h) [see also the specific example in Figure 15(a)], unless stated otherwise. Focusing on the two key application areas of power electronics mentioned above (grid interfaces and motor drives), this article gives an overview on converter families that will benefit from MBDSs and briefly discusses most recent MBDS device concepts.

Three-Phase Grid Interfaces

Three-phase ac–dc grid interfaces are widely used in generic power supply applications (e.g., telecommunication equipment, etc.) or, as shown in Figure 3, for EV battery charging. Typically, galvanic isolation is realized with a dedicated isolated dc–dc converter stage [Figure 3(a)],

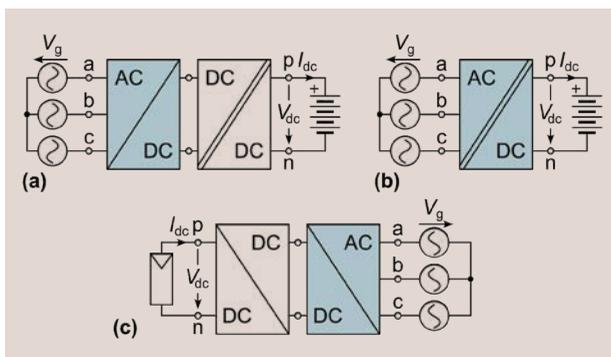


FIG 3 Examples of three-phase grid interfaces. (a) Non-isolated ac–dc rectifier with a dc–dc isolation stage or (b) isolated single-stage ac–dc converter for EV battery charging. (c) Non-isolated dc–ac grid interface with opposite power flow direction for connecting a PV plant to the three-phase mains.

or, alternatively, it might be integrated into the grid interface, which then realizes single-stage isolated ac–dc conversion as shown in Figure 3(b). In both cases, bidirectional power flow capability may or may not be required. Finally, dc–ac grid interfaces connect renewable energy sources such as PV to the mains [Figure 3(c)] and thus provide power flow from the dc to the ac side. Various converter topologies for such three-phase grid interfaces will strongly benefit from the availability of MBDSs, as will be outlined in the following.

Third-Harmonic-Injection Rectifiers

The simplest way of realizing unidirectional ac–dc conversion is a passive diode rectifier. However, the resulting low-frequency mains current distortions are usually not acceptable. The integrated-active-filter (IAF) rectifier [4] shown in Figure 4(a) extends the diode bridge by a high-frequency-(HF)-operated bridge-leg, an inductor, and three phase-selector BDSs operated at mains frequency, which allows to inject a third-harmonic current into the phase with the lowest voltage (absolute value) and hence achieve sinusoidal grid currents and power factor correction (PFC) functionality. The dc output voltage, however, is defined by the difference of the maximum and the minimum grid phase voltages and hence not controlled. Output voltage control could be achieved by connecting a buck converter stage, or, advantageously, by integration of that buck stage and the IAF’s HF-operated bridge-leg, which results in the Swiss rectifier [5] shown in Figure 4(b). Whereas the Swiss rectifier is a buck-type ac–dc converter, i.e., the dc output voltage cannot exceed $V_{dc} \leq \sqrt{2/3} V_{g,ll}$ ($V_{g,ll}$ is the rms line-to-line grid voltage), a complementary, i.e., a boost-type ($V_{dc} \geq \sqrt{2} V_{g,ll}$) version can be realized [6], too, as shown in Figure 4(c).

Vienna Rectifier/T-Type Inverter

In the IAF rectifier, the grid voltage defines the conduction state of the diode bridge (i.e., it is line-commutated) and hence the dc output voltage. Shifting the IAF rectifier’s inductor to the ac side (one per phase) decouples the diode bridge from the grid and hence allows to define its switching state using the phase-selector switches (i.e., it is forced-commutated) that are then directly connected to a capacitive dc-link midpoint. The resulting Vienna rectifier (VR) topology [1] mentioned above and shown in Figure 5(a) thus achieves sinusoidal grid currents and a controlled dc output voltage using HF pulse-width modulation (PWM) of the phase-selector switches. The VR is a widely used boost-type PFC rectifier that advantageously features three-level bridge-legs (each switch-node can be connected to p, n or m, depending on the switching state and the phase current direction) and thus reduced grid-side filtering effort. Note that the MBDSs need to block only half of the total dc output voltage, which, e.g., allows to use ± 600 V GaN MBDSs in a VR interfacing a 400 V grid to an 800 V dc output [7]. Alternatively, the

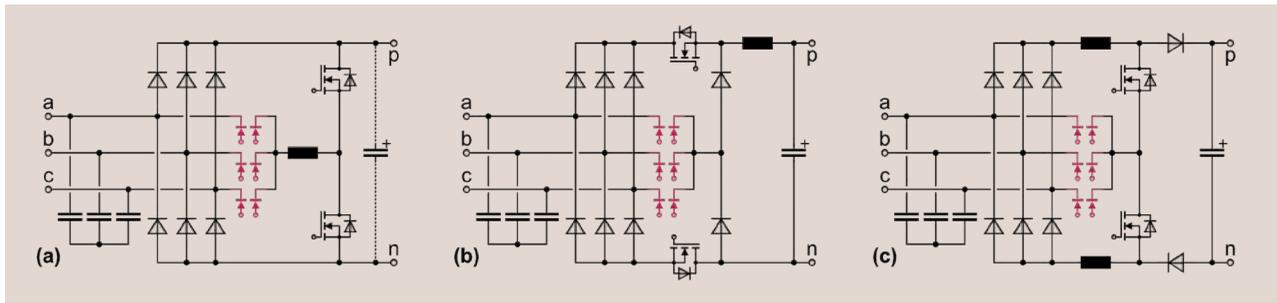


FIG 4 Third-harmonic-injection rectifiers. (a) Integrated-active-filter (IAF) PFC rectifier without dc voltage control [4]. (b) Swiss rectifier [5] and (c) its boost-type variant [6].

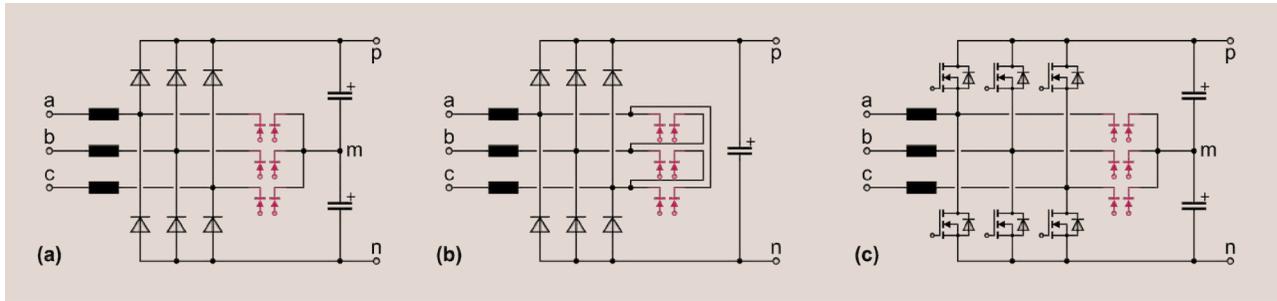


FIG 5 (a) Vienna rectifier (VR) [1]. (b) Delta-switch rectifier [8]. (c) Bidirectional three-level T-type rectifier/inverter [7], [9].

delta-switch rectifier [8] shown in Figure 5(b) does not require a dc-bus midpoint connection but stresses the MBDSs with the full dc output voltage. Finally, the VR diodes can be replaced by transistors (rated for the full dc output voltage) to obtain the well-known T-type [7], [9] structure from Figure 5(c), which supports bidirectional power flow.

Three-Phase Buck–Boost PFC Rectifiers

Typical EV battery voltage ratings vary between 400 and 800 V, and the actual battery voltage changes with the state of charge. Therefore, universal EV battery chargers must provide a wide dc output voltage range, e.g., from 200 to 1000 V as indicated in Figure 6(a). This wide output voltage range must typically be provided by the ac–dc grid interface (at least partly if an isolated dc–dc converter with a certain regulation capability is employed, fully in case of emerging non-isolated EV chargers), i.e., it must provide buck–boost functionality. A first option to achieve this is the combination of a boost-type PFC rectifier, specifically a (bidirectional) VR, and a buck-type three-level dc–dc stage as shown in Figure 6(b).

The VR is a voltage-source rectifier (VSR), i.e., it features a dc-link capacitor providing a constant voltage for the converter bridge-legs. Intuitively, it can be expected that a dual topology, i.e., a current-source rectifier (CSR) with a constant dc-link *current* exists, too. The duality relationship between the two topologies has been formally described on the switch and topology level [10], [11] and Figure 6(c) shows, as an example, the duality between the MOSFET switching element used in VSRs and its dual, a series connection of a transistor and a

diode providing bipolar voltage blocking but only unidirectional current conduction capability. A dual-gate MBDS provides additional flexibility, especially bidirectional current conduction. This is required in the CSR-based buck–boost topology [12] shown in Figure 6(d) if bidirectional power flow should be supported and hence, due to the fixed polarity of the dc output voltage, both dc-link current directions are needed. Note that the main magnetic components (i.e., the dc-link inductor and the first-stage common-mode filter inductor) can be shared between the CSR and the dc–dc converter stage, facilitating improved power density and reduced implementation effort compared to the boost–buck VSR topology. On the other hand, the buck–boost CSR’s MBDSs must block the grid line-to-line voltage, i.e., ± 900 or ± 1200 V devices are needed for 400 V grid applications (compared to the ± 600 V rating of the VR’s MBDSs mentioned earlier).

Isolated Three-Phase Grid Interfaces

The fully symmetric (if realized with MBDSs) structure of the CSR stage discussed above opens the possibility of advantageously integrating galvanic isolation into the ac–dc stage [see also Figure 3(b)], resulting in the isolated single-stage matrix-type ac–dc dual active bridge (DAB) converter [13], [14] shown in Figure 7(a). The CSR stage can synthesize an amplitude-modulated (six-pulse shape) primary-side HF transformer voltage from sections of the line-to-line voltages and employ the freewheeling state to compensate for that amplitude variation. Like a DAB, the CSR stage thus shapes the transformer current together with the secondary-side full-bridge to realize a desired

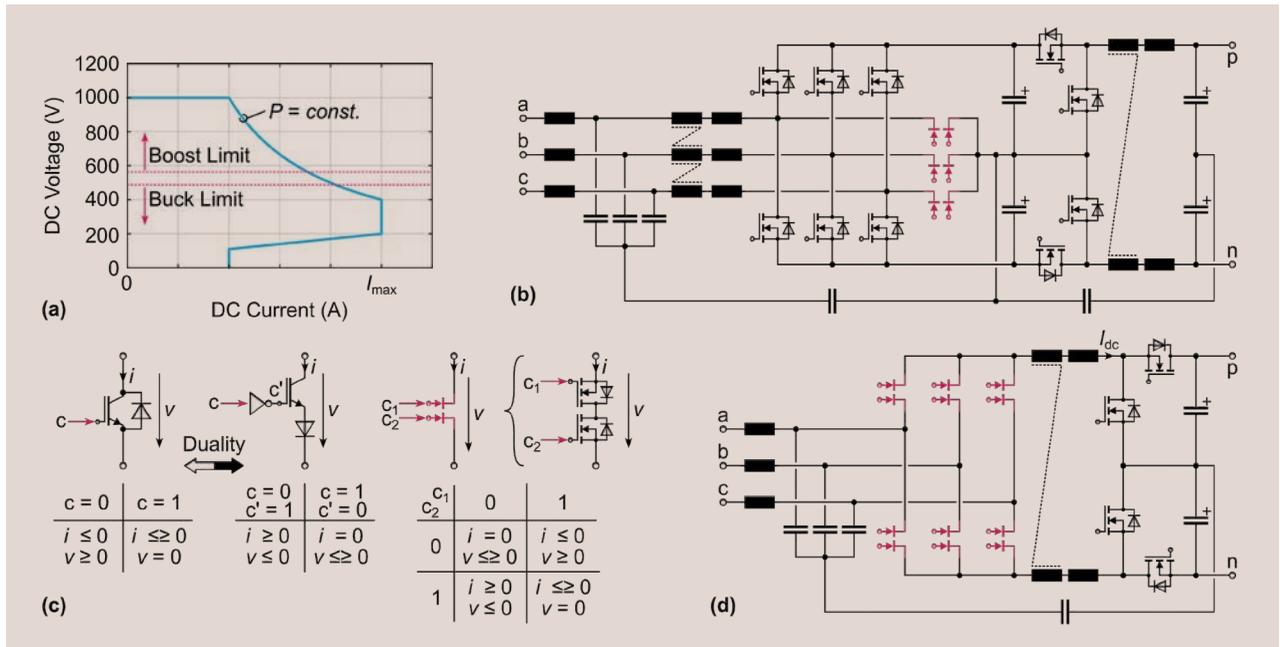


FIG 6 (a) Output voltage/current operating range for general purpose EV charger modules, indicating the need for buck-boost functionality of the grid interface. (b) Voltage-source boost-buck rectifier based on a (boost-type) VR and a buck-type three-level dc-dc stage. (c) Duality relation [10], [11] between a switching device with unipolar blocking and bidirectional current conduction capability and one with bipolar voltage blocking but unidirectional current conduction capability; a dual-gate MBDS can mimic both functionalities. (d) Current-source buck-boost rectifier topology [12], i.e., a buck-type current-source rectifier combined with a three-level boost-type dc-dc converter; note the advantageous sharing of the main magnetic components between the stages.

(constant) power transfer while achieving optimization targets such as minimum rms current or soft-switching of the power semiconductors. Finally, the CSR stage's switching sequences ensure that in each switching period the HF transformer current is distributed to all three input phases such that sinusoidal local average grid currents and thus a constant three-phase power flow result. Note that also variants of the VR with integrated galvanic

isolation exist, e.g., the Vienna rectifier II [15] with unidirectional power flow capability as shown in Figure 7(b).

Single-Phase Grid Interfaces

Allow a brief digression from the article's focus on three-phase systems: there are, of course, also single-phase grid interfaces that benefit from MBDSs. For example, the isolated matrix-type ac-dc DAB topology from Figure 7(a) can also be realized with a single-phase ac interface [16]. Regarding single-phase PV microinverters, *non-isolated* topologies are of high interest due to high efficiency and comparably lower realization effort. However, suitable topologies should not generate a HF common-mode (CM) voltage at the dc output terminals, which would drive significant leakage currents through the PV panel's relatively large earth capacitance. The Highly Efficient and Reliable Inverter Concept (HERIC) [17] shown in Figure 8 uses an ac-side BDS switch, operated at the mains frequency, to realize the freewheeling states needed for the sinusoidal shaping of the grid current, which ultimately eliminates any HF CM voltage at the dc output terminals.

Motor Drive Systems

Variable-speed drives (VSDs) are a second key application area of power electronics. As mentioned earlier, VSDs are used, e.g., to efficiently drive simple pump and blowers under varying load conditions, in EV traction chains, and in highly dynamic industry automation and robotics applications. Wide-bandgap (WBG) power semiconductors have the potential of significantly improving the efficiency of

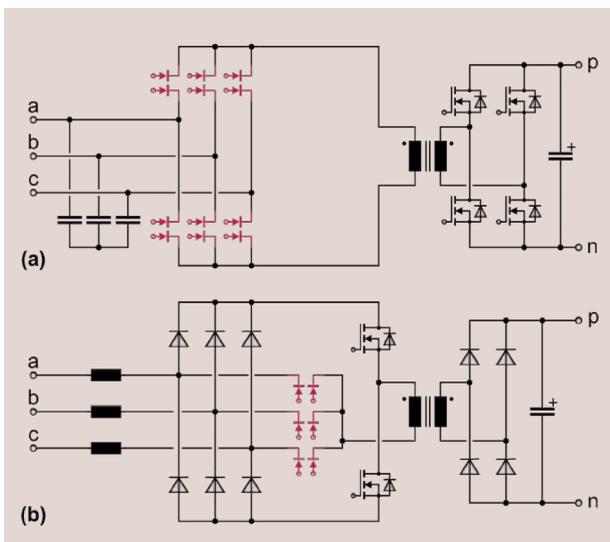


FIG 7 (a) Bidirectional matrix-type ac-dc dual active bridge (DAB) converter [13], [14]. (b) Unidirectional Vienna rectifier II [15].

such motor drive systems, however, at the price of inherently steeper slopes of the switched voltages (higher dv/dt). Therefore, WBG-based VSDs must typically be equipped with output filters to achieve motor-friendly continuous output voltages (or at least dv/dt -limitation), which prevents issues such as reflections on long motor cables and resulting transient overvoltage isolation stresses, HF common-mode ground currents that degrade bearing lifetime, and it facilitates electromagnetic compatibility (EMC) without the need for expensive shielded motor cables. As WBG devices allow much higher switching frequencies, the output filters can be comparably small. It has been demonstrated that the overall efficiency of a GaN-based drive system with LC output filter is higher than that of a conventional IGBT-based drive system without output filter [18], also due to the lower harmonic motor losses resulting from the GaN-based drive's smooth sinusoidal output voltages. Finally, there is a clear trend towards integrating VSDs directly with the motor [19] to simplify the interfaces and facilitate plug-and-play capability, i.e., high compactness and high efficiency due to typically constrained cooling possibilities in close proximity to the motor are further key features of future VSDs. Figure 9 gives a conceptual overview on typical motor drive configurations, i.e., dc-ac inverters, possibly with buck-boost functionality when operating from batteries or fuel cells, and grid-connected ac-ac VSDs. Again, for all cases with their partly differing requirements there are converter topologies that require BDSs and hence will significantly benefit from the availability of MBDSs.

DC-AC Motor Drive Inverters

Figure 10(a) shows a voltage-source inverter (VSI) with an LC output filter to achieve smooth sinusoidal motor voltages. Note that the basic VSI topology is limited to buck operation, i.e., the peak motor line-to-line voltage cannot exceed the dc input voltage. However, if the VSD operates from a battery or a fuel cell, which show significant voltage variation depending on the state of charge or the load current, buck-boost functionality might be required to always provide sufficiently high output voltages for operating the motor over the full speed range. Thus, the VSI could be complemented by a dc-dc boost stage as shown in Figure 10(b). Note that three-level topologies, i.e., bidirectional versions of some of the rectifier topologies discussed above, could be employed, too, e.g., the T-type topology from Figure 5(c) or, including the dc-dc stage, from Figure 6(b).

On the other hand, current-source inverters (CSIs) as shown in Figure 10(c) require BDSs but inherently provide sinusoidal output voltages with only a single main magnetic component (the dc-link inductor) [19], [20]. Further, a dc-dc buck input stage is required to generate the dc-link current from the available dc input voltage (shared bus, battery, etc.), i.e., the topology inherently features buck-boost capability. Note that the dc-dc stage can advantageously shape the dc-link current such that the CSI stages'

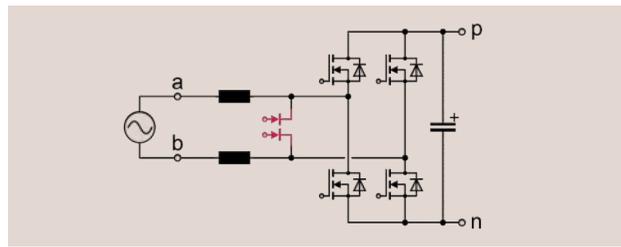


FIG 8 Highly Efficient and Reliable Inverter Concept (HERIC) for single-phase non-isolated PV inverters [17].

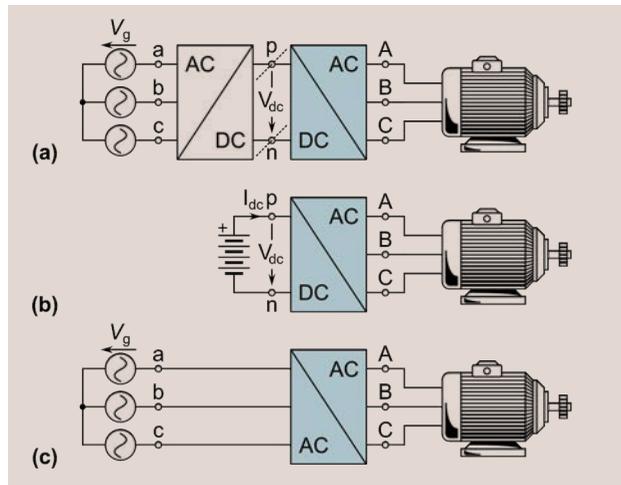


FIG 9 Variable-speed drive (VSD) system concepts. (a) Motor inverter operating from a (shared) dc bus. (b) Operating from a battery (or a fuel cell) with a strongly load-dependent dc voltage requires a dc-ac inverter with buck-boost functionality. (c) Grid-connected ac-ac VSD.

switching losses are minimized by clamping one phase at all times (synergetic control of the two stages) [20].

AC-AC Motor Drives

Thyristor-based line-commutated inverters (LCI), as shown in Figure 11(a), have been used in ac-ac motor drives since the 1970s and, typically in the megawatt power range, still are today. However, as the name implies, LCIs rely on externally defined ac voltages for the commutation of the thyristors, i.e., they only work with synchronous machines and the switching frequency is fixed by the grid/motor fundamental frequencies. Modern power semiconductors with turn-off capability facilitate current-source converters (CSCs, i.e., back-to-back connections of a CSR and a CSI with a shared dc-link inductor) with PWM operation of the rectifier and the inverter stages, resulting in advantages such as smaller dc-link inductors, higher control bandwidth, and improved harmonic performance [21]. However, note that unlike bidirectional CSRs, where the polarity of the dc-side voltage is fixed due to the dc output, ac-ac CSCs can process both power flow directions with the same, fixed dc-link current direction (note also the LCI's thyristors) by simply changing the polarity of the dc-side voltages of their CSR and CSI stages.

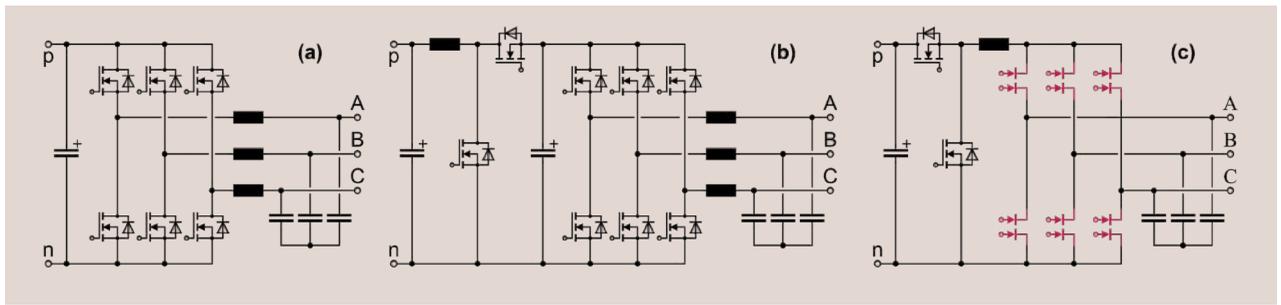


FIG 10 Motor drive inverters operating from a (possibly shared) dc bus [see Figure 9(a) and (b)]. (a) Voltage-source inverter (VSI) with LC output filter and thus sinusoidal motor voltages. (b) VSI with a dc-dc boost input stage to achieve boost-buck functionality. (c) Current-source inverter (CSI) with inherently sinusoidal output voltages and buck-boost functionality (note that the dc-dc buck stage is needed for voltage-to-current conversion).

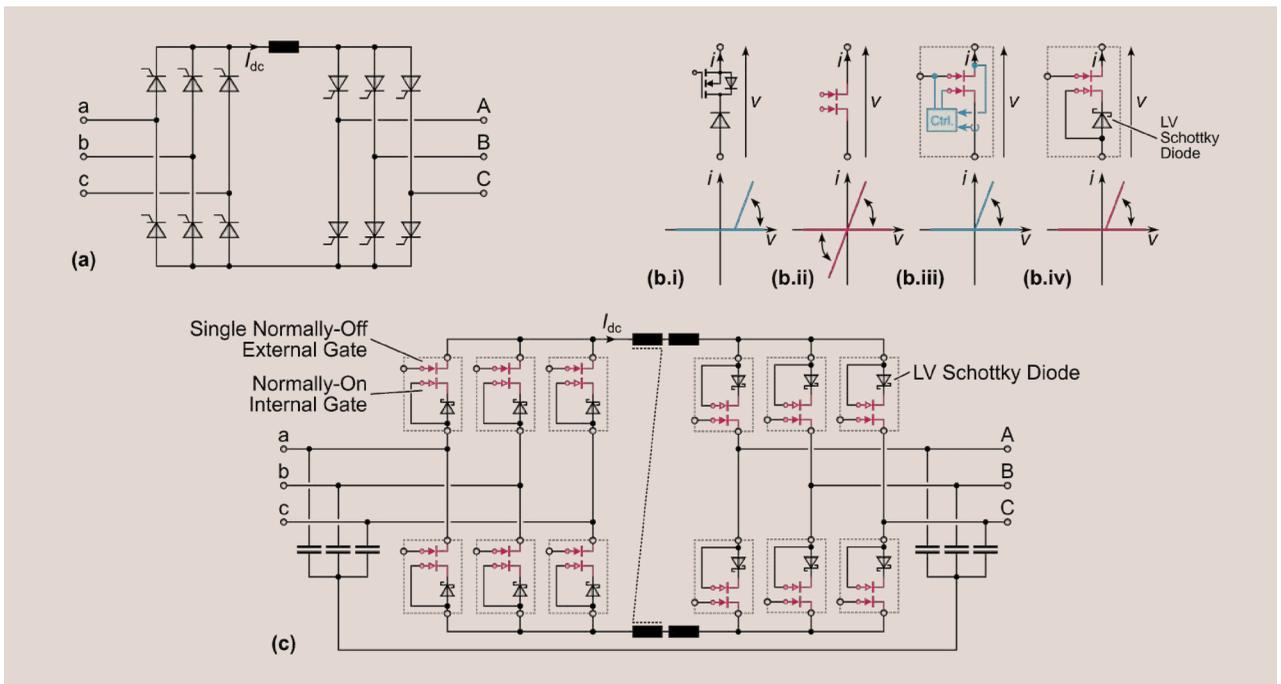


FIG 11 (a) Motor drive based on line-commutated inverters (LCI). (b) Realization of the minimum required functionality (bipolar voltage blocking but only unidirectional current conduction) for ac-ac current-source converters (CSCs) without the drawback of (b.i) a high-voltage series diode by using (b.ii) MBDSs and, to reduce complexity, (b.iii) advanced self-switching gate drives [23] or (b.iv) a cascode configuration of a MBDS and a low-voltage Schottky diode (self-reverse-blocking MBDS, SRB-MBDS) [22]; (c) SRB-MBDS-based ac-ac CSC.

Therefore, the full functionality of a dual-gate MBDS is not strictly needed, but only that of a transistor with a series diode [see Figure 11(b)]. Advantageously, this reduces the number of individual gate control signals and the overall complexity, as the commutation sequences can be simplified (no four-step commutations necessary, see below). However, a dedicated series diode needs to support the full voltage and hence shows high conduction losses. Instead, the advantageous ohmic conduction characteristic of the MBDS could be retained by controlling one of the MBDSs two gates *locally* to mimic the diode behavior (synchronous rectification), which requires a gate drive with corresponding sensing capabilities [23]. Alternatively, a cascode arrangement of a

MBDS (featuring one normally-on gate) and a low-voltage Schottky diode can provide the same functionality without sensing electronics, i.e., it achieves a self-reverse-blocking (SRB) behavior and a quasi-ohmic conduction characteristic [22]. The resulting ac-ac CSC VSD topology is shown in Figure 11(c) and features the same number of gate control signals as its dual, the ac-ac voltage-source converter (VSC) shown in Figure 12(a), but again benefits from the lower number of main magnetic components which are advantageously shared between the two converter stages. Note that higher performance (i.e., no conduction loss contribution from a low-voltage Schottky diode, small as it may be) can be achieved by accepting the higher complexity resulting from directly using dual-gate

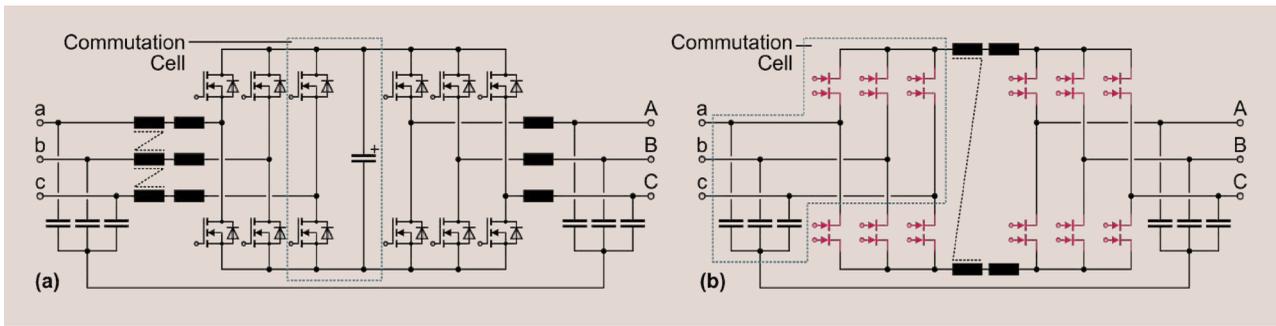


FIG 12 Core stages of ac-ac VSDs (the full grid-side EMI filters are not shown). (a) Voltage-source converter (VSC) with first-stage input and output common-mode (CM) and differential-mode (DM) filters, and boost-buck functionality. (b) Current-source converter (CSC) with MBDSs, integrated first-stage CM and DM filters, and buck-boost functionality. Note that a CSC commutation cell comprises three MBDSs and that the main magnetic components are shared between the converter stages.

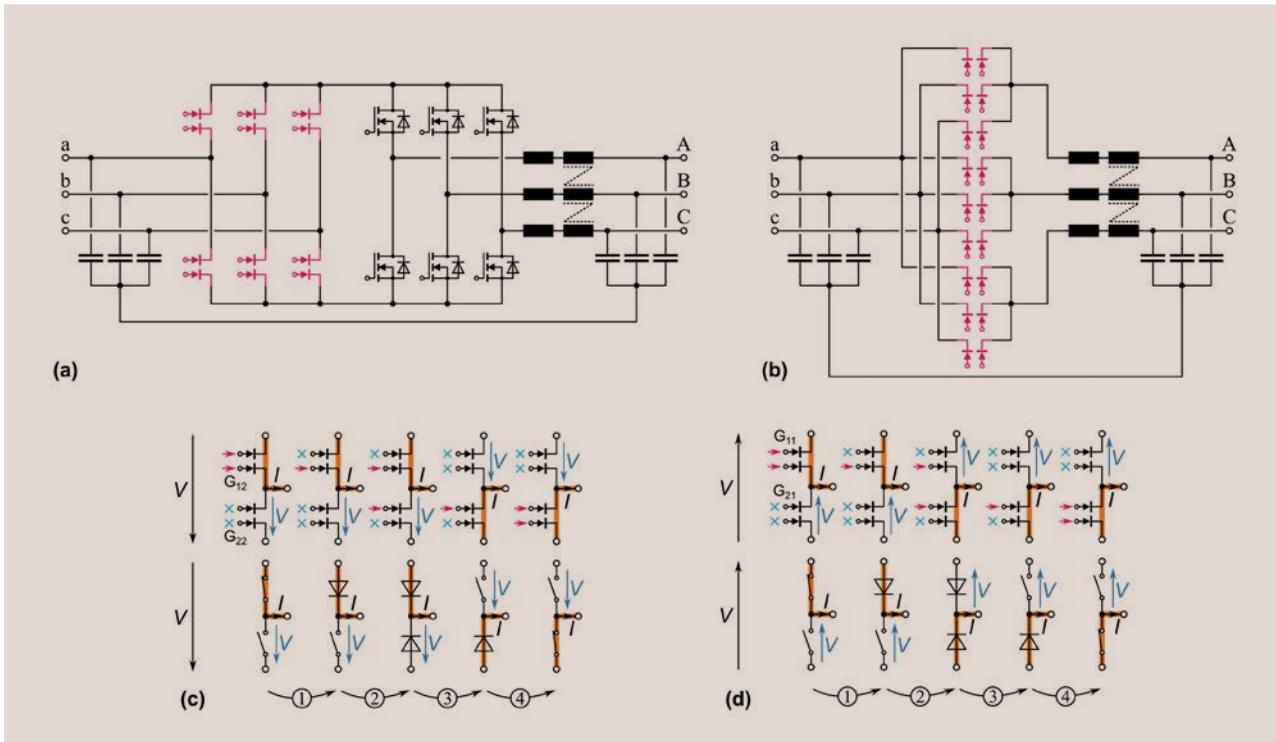


FIG 13 VSDs based on ac-ac matrix converters. (a) Indirect matrix converter (IMC) [24], i.e., a back-to-back configuration of a current-source rectifier (CSR) and a voltage-source inverter (VSI) without intermediate energy storage elements. (b) Direct matrix converter (DMC) [2], [3] obtained from merging the IMC's two stages, achieving ac-ac conversion with the minimum of only nine BDSs. (c) and (d) show current-direction-dependent four-step commutation sequences [25] for DMCs [and also for CSC commutation cells, see Figure 12(b)] using dual-gate MBDSs; the second row shows the functional equivalent circuit for each step. Note that safe commutations are achieved regardless of the applied voltage polarity.

MBDSs as shown in Figure 12(b). In the future, however, this perceived complexity increase might become irrelevant with further integration of MBDSs, gate drives, and possibly sensing electronics and commutation logic into intelligent CSR/CSI commutation cell modules.

As the instantaneous power flow of (symmetric) three-phase systems is constant, it is in principle not necessary to provide an energy buffer (capacitor, inductor) in the dc-link of an ac-ac VSD. Omitting this energy storage element is the key idea of matrix converters such as the indirect matrix converter (IMC) [24] shown in Figure 13(a),

i.e., a back-to-back arrangement of a CSR and a VSI, featuring a voltage dc-link with strictly positive voltage but without an energy storage capacitor. The two converter stages can be integrated, resulting in the direct matrix converter (DMC) [2], [3] that realizes ac-ac conversion with a minimum of only nine BDSs, as shown in Figure 13(b). Both topologies, IMC and DMC, are limited to buck operation; specifically, the maximum motor voltage V_m is limited to $V_m \leq \sqrt{3/2} \cdot V_g \approx 0.86 V_g$, where V_g is the grid voltage. Note further that the DMC [and, for that matter, also the commutation cells of CSCs, see Figure 12(b)]

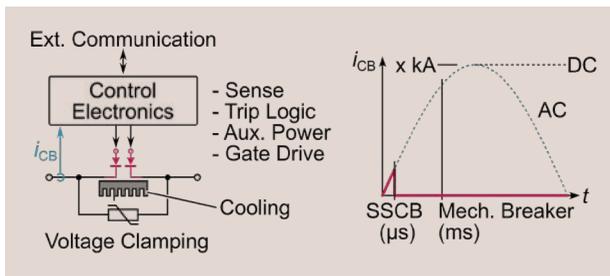


FIG 14 Key components of an ac solid-state circuit breaker (SSCB) realized with an MBDS and comparison of the reaction times between an SSCB and a conventional mechanical circuit breaker, see also [29].

require multi-step commutation sequences to ensure that there is always a path for the inductor current while never short-circuiting any of the capacitors. Typically, four-step commutation sequences that depend on the current direction [Figure 13(c) and (d)] [25] or on the voltage polarity [26] are employed; but also variants with fewer steps have been described. Clearly, the availability of MBDSs renders the DMC topology a highly attractive realization option for ac-ac VSDs due to the minimal switch count. Thus, for example, a GaN MBDS-based DMC achieving extreme compactness by massive on-chip/in-PCB integration has been demonstrated in [27], and [28] describes a

Monolithic Bidirectional Switch Concepts

It is beyond the scope of this article to provide a comprehensive history of the MBDS development. Thus, suffice to say that early activities regarding MBDS semiconductor realizations can be traced back to the turn of the millennium, where not only reverse-blocking IGBTs (RB-IGBTs) [33] have been demonstrated, but also early MBDS concepts [34]. A few years later, various companies started to investigate MBDSs based on GaN HEMTs featuring two individual gates and especially a shared drain region that is used for blocking either voltage polarity [35], [36], [37], [38]. Thus, GaN MBDSs can be considered the most mature MBDS technology, with ± 600 V, 140 m Ω samples being available [7], [38]. Figure 15(a) shows a schematic device cross section of such a normally-off dual-gate GaN MBDS (gate-injection transistor, GIT); alternative realizations feature normally-on gates or cascode configurations with LV MOSFETs connected in series with either source terminal [39].

SiC-based MBDSs have been demonstrated recently, too, which would allow for increased blocking voltages above the ± 650 V typically achieved with GaN-based lateral device concepts. Figure 15(b) shows a BiDFET [40], a monolithic (in the sense of on-chip) arrangement of two SiC transistors with integrated JBS diodes. Whereas the BiDFET provides a blocking voltage of ± 1200 V, it is essentially a common-drain arrangement of *two* transistors and hence there are *two* drift regions, one for supporting each blocking voltage polarity. Thus, whereas there are benefits from the on-chip inverse-series connection, e.g., regarding handling and packaging, the factor-of-four penalty in chip area usage [see Figure 2(g)] still applies. The same is true for a vertical back-to-back configuration of two MOSFET dies with a metal interposer layer in-between [41], see Figure 15(c). This is in contrast to the true monolithic bidirectional 4H-SiC IGBT device [42] shown in Figure 15(d), where the shared drain region is clearly visible; initial prototype devices achieved measured blocking voltages of up to ± 7 kV. Such vertical SiC MBDS concepts, however, require non-standard double-sided lithography processes and are more challenging to cool as both sides of the wafer feature intricate structures (gates, etc.). Finally, Figure 15(e) shows a recently demonstrated true monolithic bidirectional Si bipolar junction transistor (BJT) with a shared collector region (B-TRAN) [43]. The devices achieve a blocking voltage of ± 1200 V and support pulsed currents of up to ± 100 A, but, being BJTs with a typical current gain of three to four, require relatively complex gate drive circuitry providing the corresponding base currents.

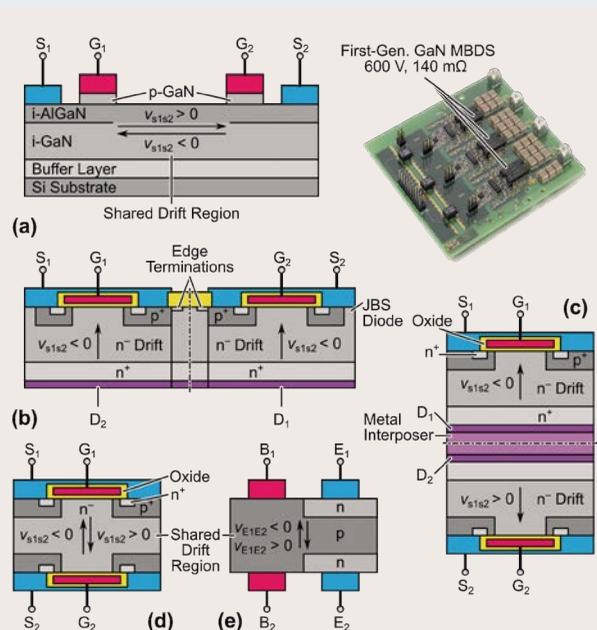


FIG 15 Conceptual (more details are given in the references) device cross sections of various MBDSs. (a) Monolithic bidirectional dual-gate GaN HEMT [35], [36], [37], [38] with a single drift region for both blocking voltage polarities, and test board with a CSC commutation cell [see Figure 12(b)] realized with first-generation ± 600 V, 140 m Ω samples [38]. (b) SiC BiDFET [40] and (c) similar vertical back-to-back connection of *two* SiC MOSFETs [41]. (d) Monolithic bidirectional 4H-SiC IGBT with a single drift region [42] and (e) B-TRAN [43], a monolithic bidirectional Si bipolar junction transistor, also with a single drift region.

2-kW ac–ac DMC operating from a 200 V grid using early discrete dual-gate GaN MBDSs.

Solid-State Circuit Breakers

Finally, MBDSs might also find use in future ac solid-state circuit breakers (SSCBs) [29]. As Figure 14 shows, SSCBs comprise in addition to the power semiconductor itself (which requires BDS capability, at least in ac applications) also an overvoltage protection element, current sensing and control electronics, and possibly an external communication interface that facilitates integration in smart grid environments or advanced remote configuration options such as dynamic adaption of trip levels or utilization as a remote-controlled load switch. Given today's sensing and processing capabilities, SSCBs can react significantly quicker than conventional mechanical circuit breakers, which implies that the switched fault current is limited to relatively low values even if the system's prospective short-circuit current is high. On the other hand, during regular operation the load current flows through the power semiconductors and generates conduction losses. Thus, MBDSs with an inherently better per-chip-area on-state resistance compared to discrete realizations [see Figure 2(g) and (h)] are thus attractive for future SSCBs [30], [31], [32].

Conclusion

Power electronics is a key enabling technology for solutions to the 21st century's major challenges such as the climate crisis. As outlined in this article, there are many converter topologies (e.g., Vienna rectifiers, current-source or matrix converters, etc.) for key application areas like grid interfaces and motor drives, which require switches with bidirectional voltage blocking and bidirectional current conduction capability, i.e., bidirectional switches (BDSs). These topologies will hence benefit from the availability of dual-gate single-drift-region MBDSs, which can overcome the factor-of-four penalty in chip area usage of conventional discrete realizations. With MBDSs removing this structural drawback, these converter topologies become regular members of the family and their suitability for many applications must be reevaluated. In addition, the emergence of MBDSs inspires the derivation of new topologies, e.g., [44].

GaN MBDSs are already quite mature and approach commercial availability, but as of now are limited to blocking voltages of up to ± 650 V. Whereas this is sufficient for three-level Vienna rectifiers or T-type converters connected to the 400 V mains, it is not for current-source or matrix converters. SiC MBDSs that would allow higher blocking voltages are considered in research, but the vertical device structures come with challenges such as non-standard two-sided wafer processing and a more complicated interface to cooling systems.

Looking at the technology S-curves of power electronics development cycles shown in Figure 16, it becomes clear that each cycle has been driven by a new power

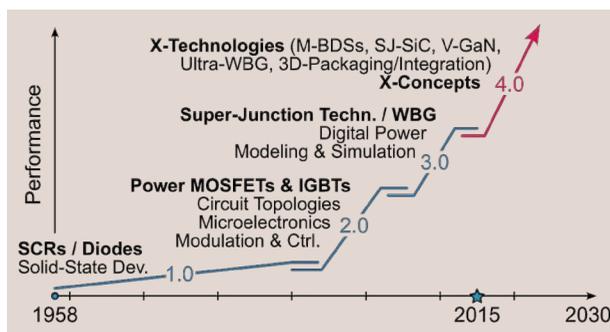


FIG 16 Technology S-curves of power electronics development cycles, typically triggered by new power semiconductor technologies. Replacement/disruptive technologies improve performance not only by a few percentage points but by factors (i.e., X-Technologies and X-Concepts [49] by a factor X).

semiconductor technology (see also [45]); most recently by the transition to wide-bandgap (WBG) devices. It can be expected that MBDSs, especially once higher blocking voltages are achieved either by improved GaN technology (e.g., 1200 V using sapphire substrates [46]) or mature SiC MBDSs, are, together with superjunction SiC devices [47], and ultra-WBG materials (like diamond) [48], amongst the X-Technologies [49] shaping the ongoing disruptive transition to Power Electronics 4.0. In addition, a further key technology will be the integration (functional and physical) of power switches (e.g., MBDSs) and surrounding circuitry (gate drives, sensing, commutation logic), aiming at masking complexity (such as four-step commutation sequences) from the application. Also, on the physical level and following trends from microprocessor technology [50], concepts for monolithic 3D-integration [27] of power, information, and cooling systems will be necessary to achieve highest performance using a minimum of space and resources.

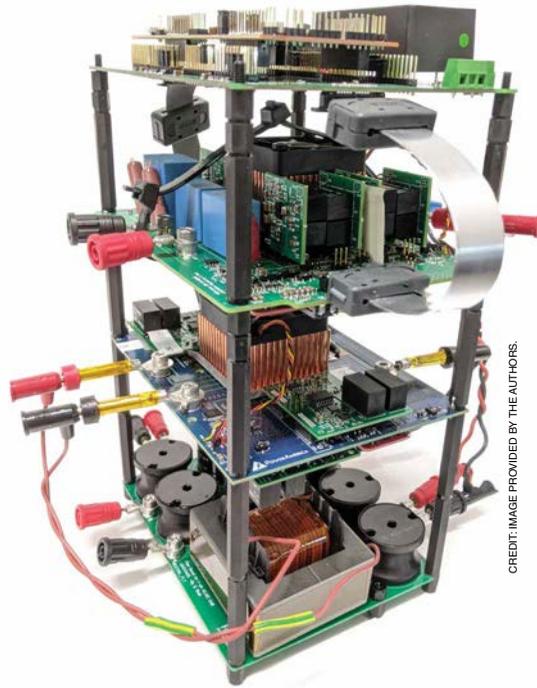
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Power Conversion Systems Enabled by SiC BiDFET Device

by Subhashish Bhattacharya, Ramandeep Narwal, Suyash Sushilkumar Shah, B. Jayant Baliga, Aditi Agarwal, Ajit Kanale, Kijeong Han, Douglas C. Hopkins, and Tzu-Hsuan Cheng

The BiDirectional Field-Effect Transistor (BiDFET) can enable circuit topologies requiring four-quadrant switches, that were earlier designed using discrete combinations of MOSFETs, IGBTs, GaN HEMTs, and PiN diodes. The monolithic nature of the BiDFET allows lower device count, smaller switch volume, lower inductance, and simpler packaging, and hence more reliable and commercially viable implementation in power electronics converters. The matrix converter topologies, now feasible using BiDFETs, can eliminate the bulky and unreliable dc link capacitors or inductors required for conventional voltage-source or current-source converters in ac-ac and ac-dc applications. The 1.2 kV BiDFET has the potential to disrupt

all the applications utilizing 1.2 kV switches, including electric vehicle (EV) drivetrain, bidirectional EV chargers, industrial motor drives, solid-state transformers, datacenter power supplies, elevator drives, dc microgrids, energy storage grid integration, solid-state breakers, etc.

Converter Topologies Using BiDFET

Converter topologies implementable using BiDFET can be categorized by identifying the converter cells used for their implementation. Four different converter cells utilizing BiDFET are shown in Figure 1(b)–(e), and Table 1 lists the popular converter topologies corresponding to each converter cell.

The BiDFET device is fabricated as a monolithic four-terminal switch comprised of two internal 1.2 kV 4H-SiC JBS (Junction Barrier Schottky)-diode-embedded-power

MOSFETs (JBSFETs) connected in a common-drain configuration [1]. Any four-quadrant switch implementation, including back-to-back connected SiC MOSFETs will require at least four semiconductor devices to achieve the same functionality. The BiDFET as a monolithic four-quadrant switch enables a converter with smaller inductance commutation cells due to a lower number of devices, no wire bonds requirement, and eventually smaller package size.

First Converter Hardware Demonstration Using 1.2 kV SiC BiDFET

A single-phase, single-stage, isolated ac–dc converter utilizing BiDFET enabled single-phase matrix converter on grid-side has been designed, developed, and implemented for solar PV applications [11] (Figure 2). This BiDFET-enabled converter presents significant improvements over conventional ac–dc isolated converters built with a dc–dc dual active bridge (DAB) cascaded with PWM inverter or folder-unfolder stage and a dc link using bulky unreliable electrolytic capacitors. The developed converter, requiring a lower number of switches and no electrolytic capacitors, presents a lower volume and higher reliability solution.

The hardware prototype is implemented as a stack of four PCBs (Figure 3). The top PCB is the control board which supplies the auxiliary power, accepts sensor signals, generates PWM gate signals, and protects the converter against faults through hardware and software trip settings. The second PCB is the grid-side full-bridge converter enabled by 1.2 kV Gen-1 SiC BiDFET with filter capacitor, C_f , and parallel $R_f - C_f$ damping branch on the same board. The third PCB

is the PV-side full-bridge converter enabled by 650 V GaN Systems' enhancement-mode GaN transistor (GS66516T). The fourth PCB is a filter and high-frequency ac-link board, which includes the grid-side inductors $L_f/2$, PV-side second-harmonic filter capacitor C_{dc} , high-frequency inductor L_r , and high-frequency transformer. The filter PCB is kept closer to the PV-side full-bridge converter PCB as it contains the capacitor C_{dc} , required to filter line-frequency second-harmonic components on the PV-side.

An algorithm incorporating all modulation strategies and operating modes of the ac–dc DAB converter is implemented for optimized converter design and modulation scheme. It leverages

Table 1. Converter topologies.

Converter cell	Converter topologies
Current-injection type	Hybrid third harmonic injection-based rectifier [2], Δ -switch rectifier [3], VIENNA rectifier [4], SWISS rectifier [5]
T-type	T-type converter [6]
Resonant type	Auxiliary resonant commutated pole (ARCP) converter [7]
Matrix type	Direct matrix converter [8], Indirect matrix converter [9], Current-source converters [10]

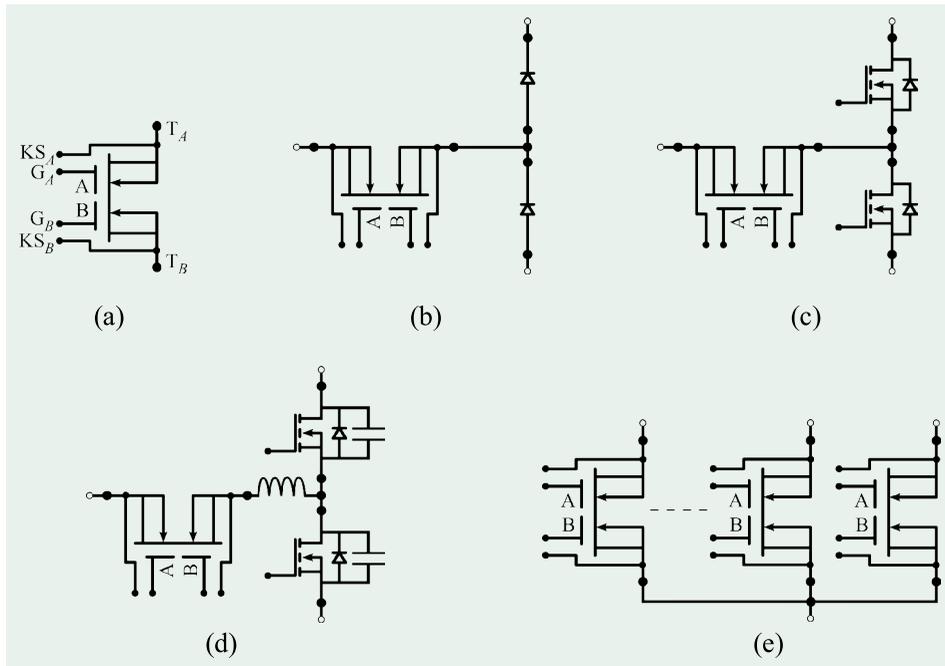


FIG 1 (a) BiDFET symbol: T_A and T_B are source terminals, G_A and G_B are gate terminals, KS_A and KS_B are kelvin source terminals, and arrows denote body diodes of the constituent JBSFETs. (b) Current-injection type converter cell. (c) T-type converter cell. (d) Resonant type converter cell. (e) Matrix type converter cell.

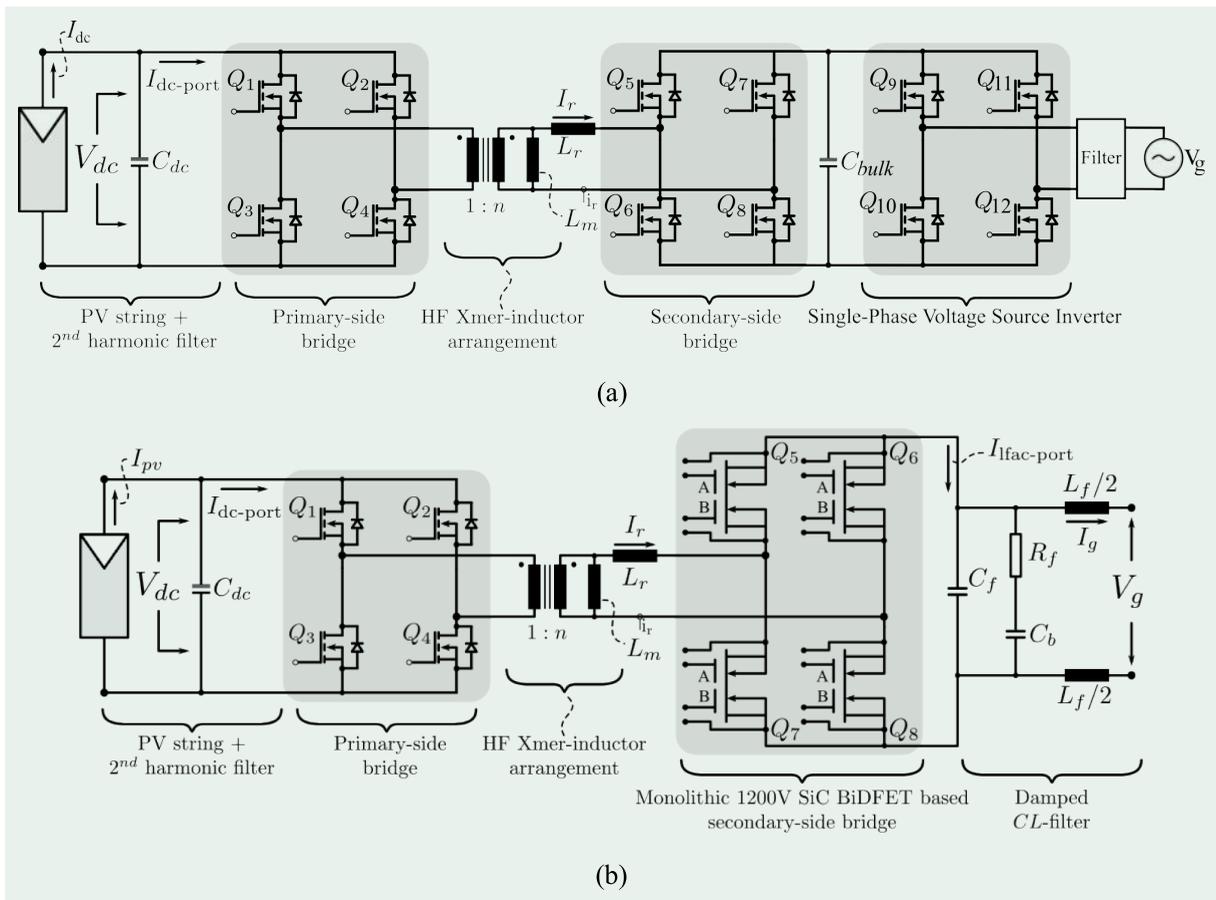


FIG 2 (a) Conventional two-stage isolated ac-dc converter with dc link. (b) Single-stage isolated ac-dc DAB converter using BiDFET enabled matrix converter on ac-side.

the three degrees-of-freedom (duty ratio of dc-side full-bridge converter output, duty ratio of ac-side full-bridge converter output, phase-shift between dc-side and ac-side full-bridge outputs) and optimizes the high-frequency RMS current, size of magnetic elements and soft-switched region of the converter. The hardware experimental results are shown in Figure 4 for 40% load and 100% load. The dead-time near the zero crossing of the ac output current enables safe commutation of the constituent FETs of the BiDFET. Even with the zero crossing distortion, the total power factor and the current THD at 100% load, as measured at the converter output by the Hioki Power Analyzer PW6001, are 0.999 and 4.7%, respectively. For further improvement of current THD, zero-crossing distortion can be reduced by employing voltage or current based four-step commutation schemes used for matrix converters.

The measured converter efficiency across the load and estimated loss distribution in different components are shown in Figure 5. These losses include the loss in the semiconductors, transformer core, transformer and high frequency inductor winding, dc side filter capacitor (high and low frequency losses), and ac side filter capacitor. The transformer and inductor were built using solid wire winding in this prototype, leading to winding losses constituting a major percentage of total losses. The converter efficiency

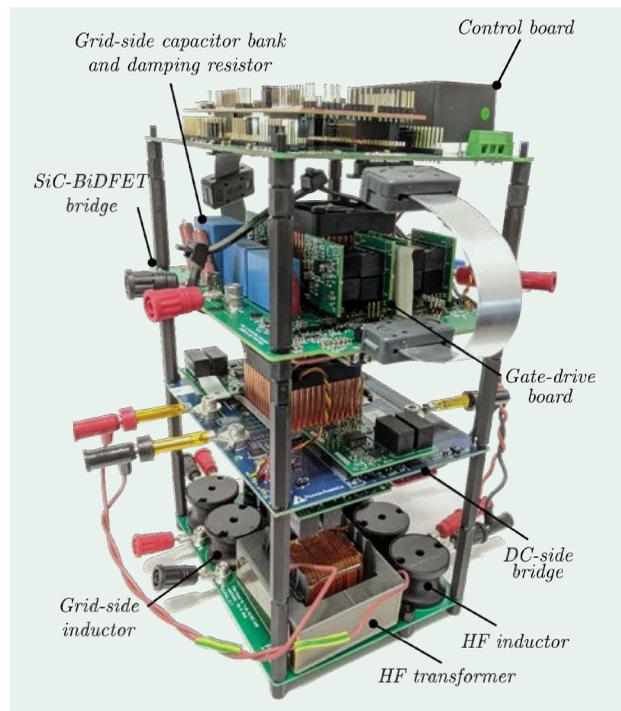


FIG 3 Hardware prototype of the 2.3 kW, 400 V to 277 V_{RMS} single-phase ac/dc DAB converter using Gen-1 BiDFET enabled matrix converter on ac side.

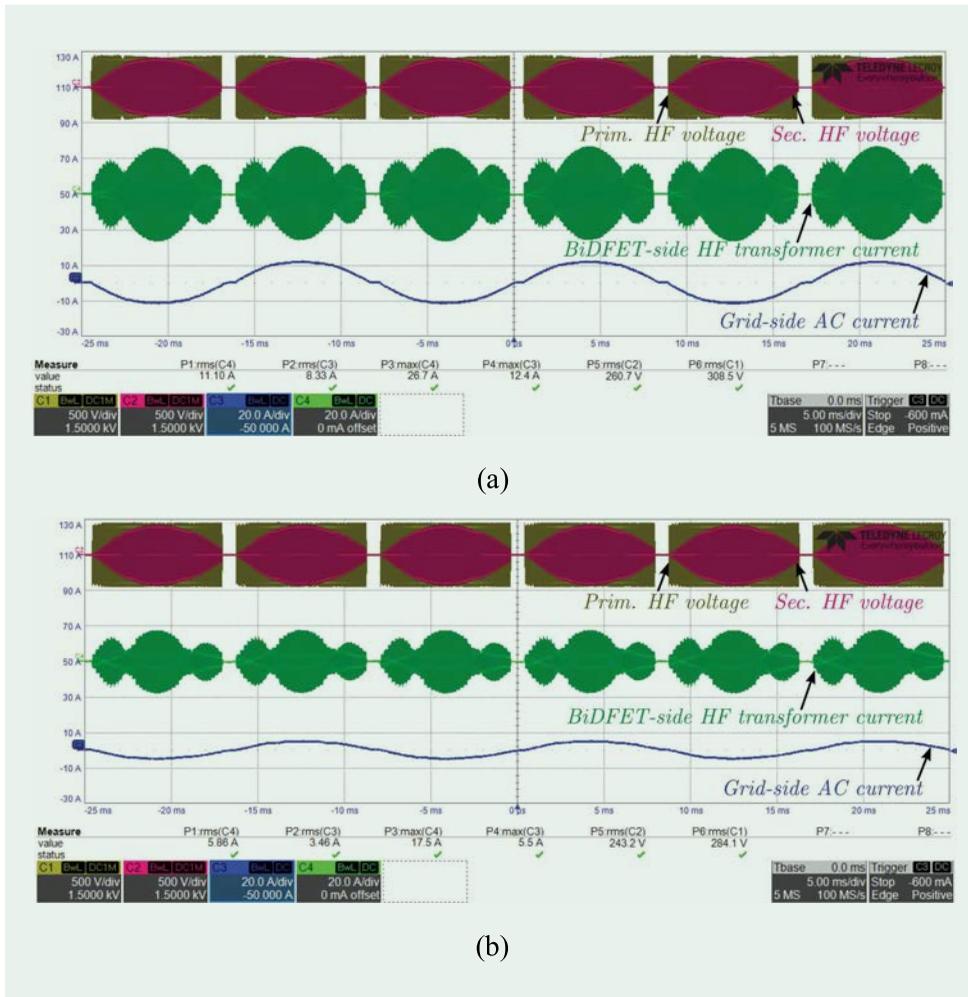


FIG 4 Operating waveforms of the 2.3 kW single-phase ac-dc converter at input dc voltage of 400 V and output voltage of 277 V_{RMS} with (a) 100% load and (b) 40% load.

can be improved by using litz wire winding for magnetic components. Assuming all losses except semiconductor loss as zero, the converter efficiency metric termed 'semiconductor efficiency' is also plotted to mark the maximum possible efficiency with selected semiconductor components. The current THD, overall efficiency, and semiconductor efficiency at 2.3 kW, 400 V_{DC} input and 277 V_{RMS} output voltage with 50 kHz switching frequency are 4.7%, 95.3% and 98.4% respectively.

The converter semiconductor efficiency can be improved further by replacing Gen-1 BiDFET with Gen-2 BiDFET in the grid-side full-bridge converter. Gen-2 BiDFET has 25 mΩ on resistance, which is around half that of the Gen-1 BiDFET, while the switching losses are almost the

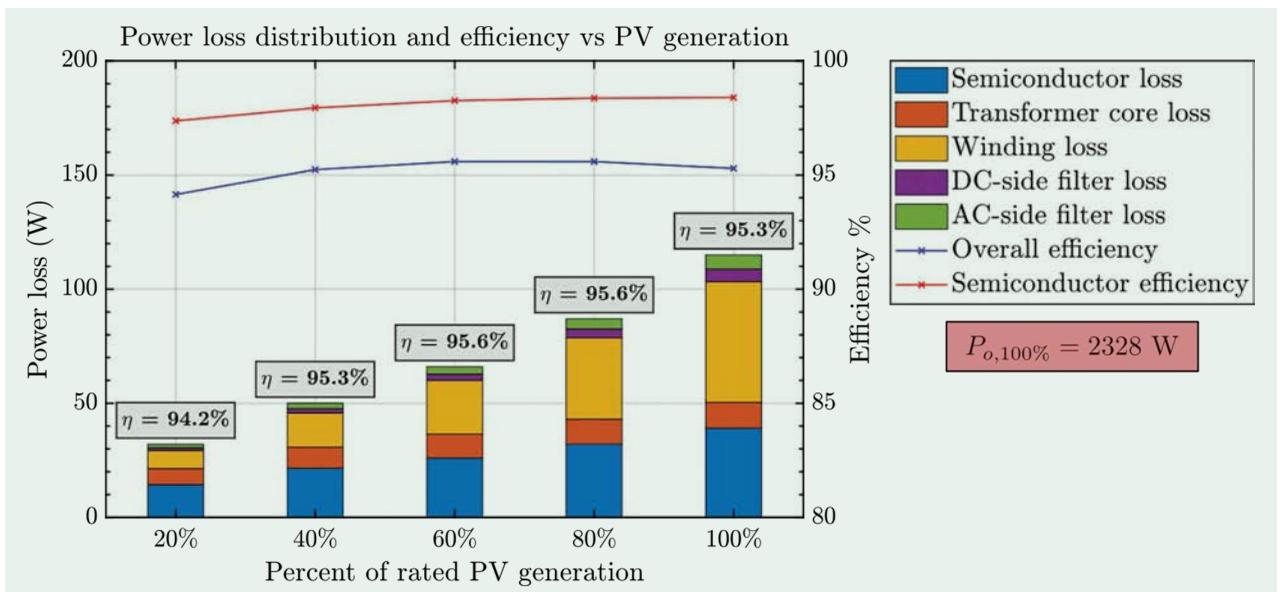


FIG 5 Single-phase ac-dc converter overall efficiency, semiconductor efficiency and estimated loss distribution at different rates of PV generation.

same for the two devices due to the same chip size. Semiconductor efficiency for single phase ac–dc converter with Gen-2 BiDFET based grid-side full-bridge is estimated to increase by 0.2%. The difference in converter semiconductor efficiencies with Gen-1 and Gen-2 BiDFET devices will increase with the increasing device operating current levels, that is, when device conduction loss becomes more significant than device switching loss.

Conclusion

The development of BiDFET as a single-chip SiC four-quadrant switch paves the way for the implementation of reliable 1.2 kV four-quadrant switches-based power conversion systems. Depending on the cooling method and desired converter efficiency, the recently developed Gen-2 BiDFET (having 25 m Ω on-resistance) can enable multiple kilowatts applications. The continuous operation of SiC BiDFET device has been demonstrated through experimental results of 2.3 kW, 400 V_{DC} input, and 277 V_{RMS} output single-phase isolated ac–dc converter.

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FEPPCON XI—Part II: Technical Committee Scope: Road Mapping Exercise

by Pat Wheeler

The IEEE Power Electronics Society (PELS) currently has twelve Technical Committees (TC) covering a range of technical and application areas of power electronic systems. The number of TCs was increased from seven to twelve in 2020, reflecting the global growth in power electronics in terms of scope and application. The TCs

provide a community home for power electronics engineers within PELS, with activities including conferences, workshops, webinars, awards, competitions, seminars, standards, tutorials and technical meetings. The twelve Technical Committees are:

- TC 1: Control and Modelling of Power Electronics
- TC 2: Power Components, Integration, and Power ICs
- TC 3: Electrical Machines, Drives and Automation
- TC 4: Electrified Transport Systems
- TC 5: Sustainable Energy Systems
- TC 6: Emerging Power Electronic Technologies
- TC 7: Critical Power and Energy Storage Systems
- TC 8: Electronic Power Grid Systems
- TC 9: Wireless Power Transfer Systems
- TC 10: Design Methodologies
- TC 11: Aerospace Power
- TC 12: Energy Access and Off-Grid Systems

In order to validate the coverage and scope of the PELS TCs, there is a PELS requirement for IEEE Future of Electronic Power Processing and Conversion (FEPPCON) to review every two years. The latest review took the form of a road-mapping workshop with all attendees writing down their key and future topics in power electronics on post-it notes and then putting these post-it on boards headed with the key words from the title of each TC. The output

of this process can be seen in Figure 1. This part of the road-mapping process was followed with discussions around each board and reflection on the process.

The results of this road-mapping process are shown in Table 1, giving each TC a view of how this particular group of power electronics engineers view their topics. This information is invaluable in terms of marketing and organisation, while highlighting areas where the title might not reflect what is actually covered by a particular TC.

Table 2 gives a list of the topics which the attendees of the road-mapping session believed are not covered by any of the PELS TCs. Some of these topics are covered by the TCs, but not well reflected in the titles. Other topics are obviously absent from our technical committees and there is a plan to reflect on these, along with the membership growth in PELS, so that further TCs can be added in the future. Example areas that might be considered include:

- Passive components
 - Applications and EMI Filters
 - Inductive/Capacitive/Virtual
- Power Converter topologies
 - Multi-level/Cellular Converters
 - DC/DC

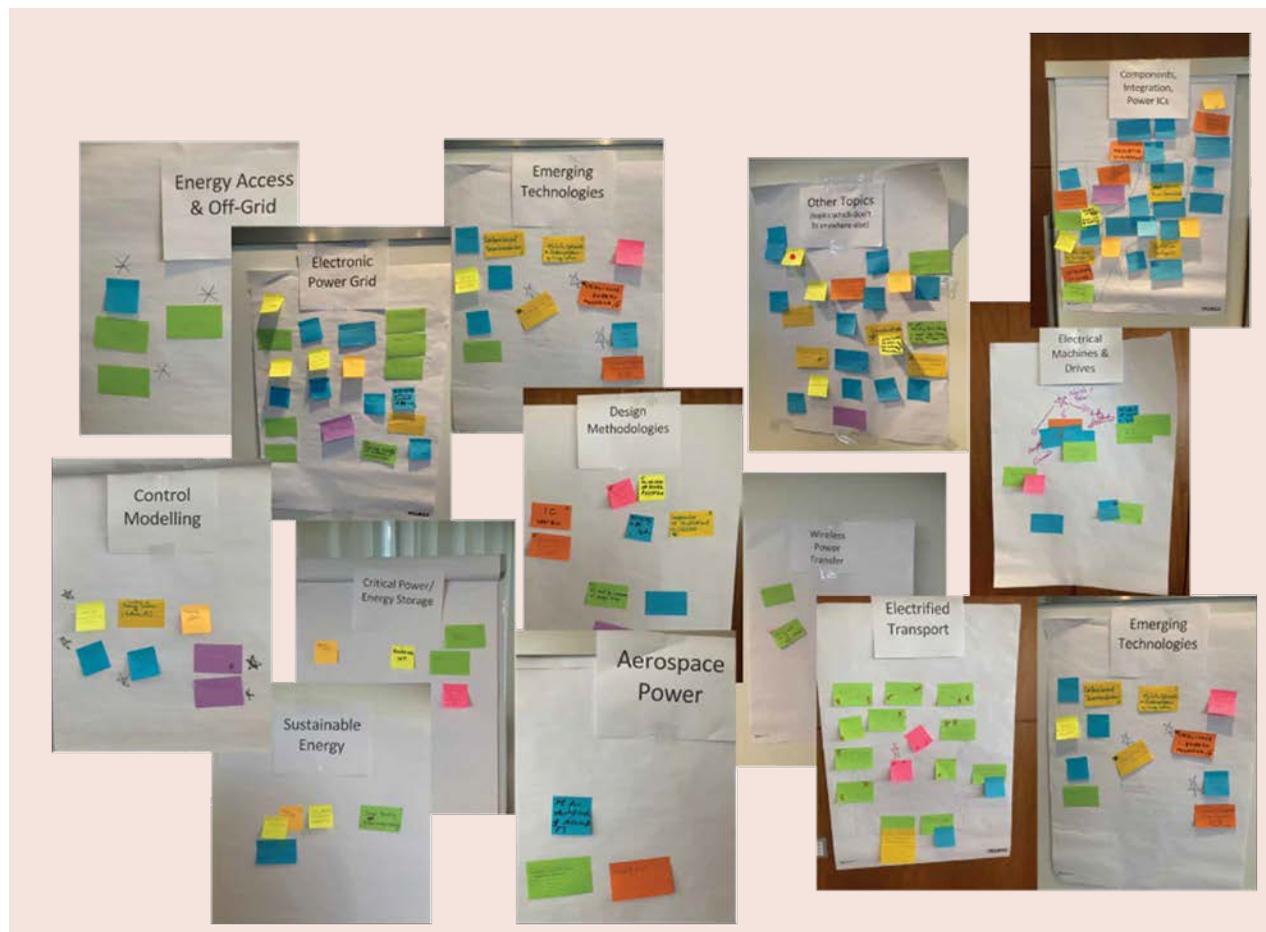


FIG 1 The output of the road-mapping session.

Table 1. Result of the road mapping exercise for each PELS TC

TC6 Emerging Technologies

- Reliability and Lifetime
- Carbon Based Semiconductors
- Holistic optimization and implementation of Energy Systems
- Compact Energy Storage solutions/design
- Sustainability of Power Electronics Technology Birth to Cradle, including recycling
- Machine Learning in Power and Electronics
- Integration with Applications
- Ubiquitous energy processing
- Integration of PE Connectivity and the circular economy.
- Artificial Intelligence and Machine Learning contexts beyond design automation
- Hydrogen Distribution System
- Thermally Regulated Power and Electronics: High Temp, Low Temp, Thermal Cycling

TC8 Electronic Power Grid

- Energy Transmission Control / Interconnect Protocols
- How to Model Power Electronic Dominated Grids
- Power Electronics for Electrical Grids
- System Integration
- Electronic Power Grid Systems
- Reliability of Power Electronic based power system
- 100% renewable energy systems built upon Power Electronics***
- Power Electronics for resistant + adaptive + sustainable grid power system.
- Microgrid – “The Grid” Requirements and Standards.
- Energy Storage and grid modernisation
- First-order analysis of cost/payback models.
- Distributed, autonomous control of Power Electronics in Grids.

TC4 Electrified Transport

- MWT Charging
- CAV Autonomous Vehicles
- Aerodynamic cool looking cost effective EVs
- Level 1 charge infrastructure (passenger cars)
- Scalable + modular + rotation drills for all EVs
- Integration compatibility cost effectiveness
- In-motion EV charging.
- High Power density traction drives
- Extreme Fast Charging
- Compliance/Reliability
- EV, Power Electronics for Transportation Electrification. // Power electrification for emergency opportunities.
- Charging access
- Electrification Transportation// electrified transportation (vehicles, power electronic drives)

TC2 Components Integration Power ICs

- Heterogeneous, Integration of Power Electronics
- 3D Embedded Power Electronics.
- Power Components (Passive/Active)/ Components.
- Magnetics (+materials)
- Change to DC distribution at least at building level.
- Integration and customization vs modernity standardization + recycling.
- low cost Power Electronics integrated, modernize.
- Power electronics for harsh Environments (Temp,....)
- New Power Devices to reduce costs
- High voltage GAN devices. (1200v and over)
- High voltage UWBG semiconductor devices.
- WBG devices and applications
- Advanced semiconductor Devices and models.
- Modular/scalable Power consumption models
- Electronic Power Processing Integration into application.
- Holistic views for system

TC3 Electrical Machines and Drives

- Integrated Motor Drives
- Miniaturization of Power Electronics (Drive on Motor)-AC Drives (integrated, new application)
- “Coupled” Thermal Management
- “Highly Coupled”-HF effects with WBG device in systems...
- Wide bandgap devices: reliability, scalability, availability.
- Motor Drives needs to be lot better.
- *Fault Diagnostics and Fault tolerance.

TC10 Design methodologies

- User Integration into designs and standards*
- Computer Aided Design of Power Systems*
- IC Designs*
- High temperature power electricity
- Reliability of PE systems
- Emphasize of verification and validation
- Power Electronics must be synonymous with energy storage.
- Standard model-mass production of power electronics.
- Data sheet Parameters.

TC1 Control Modelling

- Control of Power Electronic Systems
- Control of Energy Sources
- Modelling and Control
- Distributed Control
- Modelling of Systems
- User Interfaces
- Data Interchange, information format and content

TC5 Sustainable Energy

- Renewable energy -MAV
- Power Electronics for effective usage of electricity
- Energy affordability and Power Electronics Interoperability.
- Energy Harvesting (Ambient energy scavenging – waste energy)

Table 1. Result of the road mapping exercise for each PELS TC (Continued)

TC9 Wireless Power Transfer.		
<ul style="list-style-type: none"> Integration (+load) - deep integration of IOT enabled complete power electronic applications. Power module packaging - suitable for WBG Devices 	<ul style="list-style-type: none"> Wireless Power Transfer System Consumer and Health Care 	
TC11 Aerospace Power	TC12 Energy Access and Off Grid	TC7 Critical Power/ Energy Storage.
<ul style="list-style-type: none"> Power Electronics for Electrification of Aircraft Aerospace electrification propulsion - hydrogen Reliability of Power Electronics 	<ul style="list-style-type: none"> Power Electronics and Energy “Free” Access Emergency access at low cost Renewable energy - enabling technology Interoperability (energy access) 	<ul style="list-style-type: none"> Battery Chargers Powering the IOT Batteries: -Storage, -chargeability, environment System-level design and optimization of ESS

Table 2. Topics considered not to be covered by the existing PELS TCs

Other Topics (not seen as belonging to an existing TC)		
<ul style="list-style-type: none"> Diversity Equity Inclusion and Justice (DEIJ) in Power Electronic Society Cybersecurity Power Electronics in Healthcare Systems Power and Electronics for health/ medical applications. Power and Electronics to benefit Humanity Power density vs thermal trade-off - how to get the heat out. Reliability of Power Electronics 	<ul style="list-style-type: none"> Entire value chain -recycling -environmental treatment Sustainability and impact of Power and Electronics (Product Standards point of view) LED Lighting Standardization -standards on efficiency for consumer electronics. Educating all stakeholders on impacts today/ tomorrow of energy efficiency Biotechnology -Enable Power Electronics 	<ul style="list-style-type: none"> Active components to replace passive components. How to reduce the size of EMI filters Trust in untrusted parties. PE systems reuse + recycling DC electricity Distribution and Home Office materials Mission profiles for various applications. Power Converter Topologies. Sustainability includes cost of Power Electronic systems

- Healthcare enabled by Power Electronics
 - Bio-Technology Applications
 - Power Electronics in the Human Body
- Lifecycle Management
 - Reliability
 - Recycling and Sustainable Manufacturing

The PELS TCs are very successful in their activities and engagement, but this exercise has shown that PELS needs to continue to evolve and encourage new

application and technology areas within the power electronics discipline.

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FEPPCON XI – Part II: Reliability of Power Electronic Systems

by Huai Wang, Michael Pecht, Axel Mertens, Rik DeDoncker, and Frede Blaabjerg

To be cost effective and safe, reliability design, test and health monitoring and management are a necessary part of power electronics implementation and its integration into energy systems. Being able to design power electronics to meet a required lifetime for a given load profile with a certain probability becomes achievable as we understand the physics of failure in power electronic components much better, and as power electronic systems can be monitored, the reliability predicted and failures and malfunctions forecasted and prevented. At the “Future of Electronic Power Processing and Conversion” (FEPPCON XI) 2022, a session was held to discuss the application of state-of-the-art reliability engineering approaches—and highlight missing research areas to bring us even closer to 100% reliable power electronic products for its service life—while simultaneously it can realize

The presentation pointed out that bathtub curves are not a reality [1], failure rates are usually not constant, and Arrhenius law is often erroneously applied.

more precise predictions of the sustainability of putting a product to the market. Three presentations from leading research institutions were given at the session.

In the first presentation, Prof. Michael Pecht from the University of Maryland, MD, USA, discussed how the physics of failure and artificial intelligence (AI)

concepts can be used for qualifying electronics reliability and safety. Examples of Lithium-ion battery failure in electric vehicles (EVs) and IGBT failure in a wide range of applications were discussed. The presentation pointed out that bathtub curves are not a reality [1], failure rates are usually not constant, and Arrhenius law is often erroneously applied. Besides electrothermal stresses, water and moisture are also of considerable concern [2], [3], even in many sealed applications, in addition to electromagnetic interference (EMI). The

Center for Advanced Life Cycle Engineering (CALCE) at the University of Maryland has developed a fusion prognostic approach for remaining useful lifetime estimation [4], successfully applied for their sponsors. The presentation also emphasized the importance of

developing standards for managing reliability testing and qualification.

In the second presentation, Prof. Rik W. De Doncker from RWTH Aachen University, Germany, introduced the new research center CARL—Center for Ageing, Reliability and Lifetime Prediction of Electrochemical and Power Electronic Systems. The testing and manufacturing facilities at the center include three main areas: load and environmental simulations, construction of prototypes, and physical-electrochemical analysis. The research focuses on batteries

The testing and manufacturing facilities at the center include three main areas: load and environmental simulations, construction of prototypes, and physical-electrochemical analysis.

and power electronics. Figure 1 shows the key research topics on power electronics reliability of the research center CARL. In addition, some exemplary research projects were introduced, including ElluSense - Electroluminescence Sensing of SiC MOSFETs [5], ZuLe-SELF—Sensor technology for condition monitoring of power modules [6], NachLadBar—Sustainable vehicle charging systems, and HiEF-FICIENT—Highly efficient and reliable electric drivetrains [7]. The facility is expected to be a key research infrastructure for both

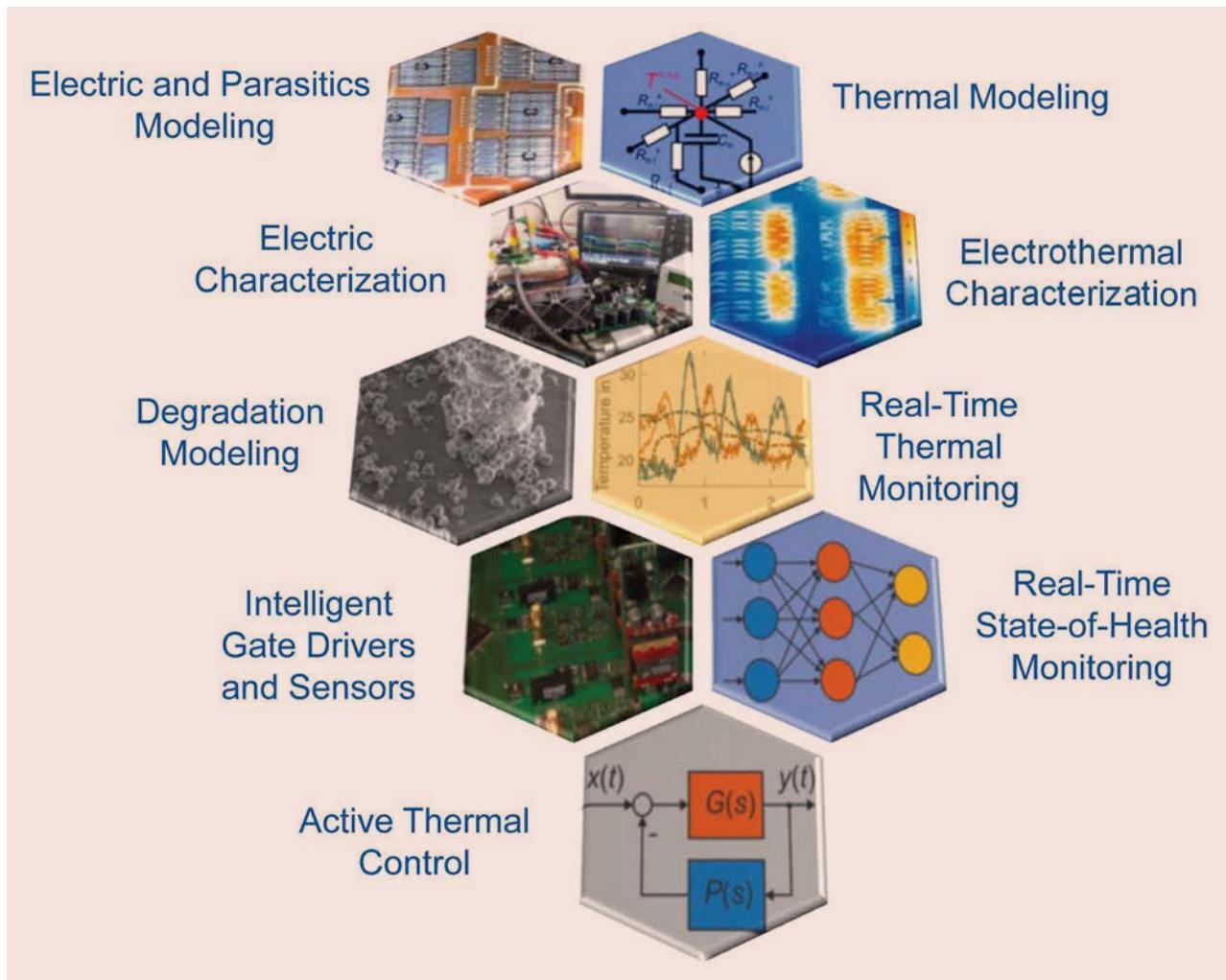


FIG 1 The research focuses on power electronics reliability of the new research center CARL—Center for Ageing, Reliability and Lifetime Prediction of Electrochemical and Power Electronic Systems. Source: Prof. Rik W. De Doncker, RWTH Aachen University.

qualifying testing and new discoveries in reliability engineering.

The third presentation was given by Prof. Huai Wang from Aalborg University, Denmark, who provided perspectives on research challenges and opportunities in power electronics reliability. It is based on a reflection of more than ten years of research activities at the Center of Reliable Power Electronics (CORPE), Aalborg University. Figure 2 shows the three main research themes on modern power electronics reliability approaches at Aalborg University, defined in 2012, covering the knowledgebase of physics of failure and physics of

Developed testing facilities for application-oriented power electronic components (e.g., power modules, capacitors, and magnetic components) and converters (e.g., photovoltaics inverters and motor drives) were introduced.

degradation, the design phase, and the operation phase.

Figure 2 also outlines six research topics for the next ten years [8]. First, the presentation discussed the unique contribution power electronic researchers can make to software reliability by investigating the interaction between software and hardware failure. Developed testing facilities for application-oriented power electronic components (e.g., power modules, capacitors, and magnetic components) and converters (e.g., photovoltaics inverters and motor drives) were introduced. Second, E-mobility and power

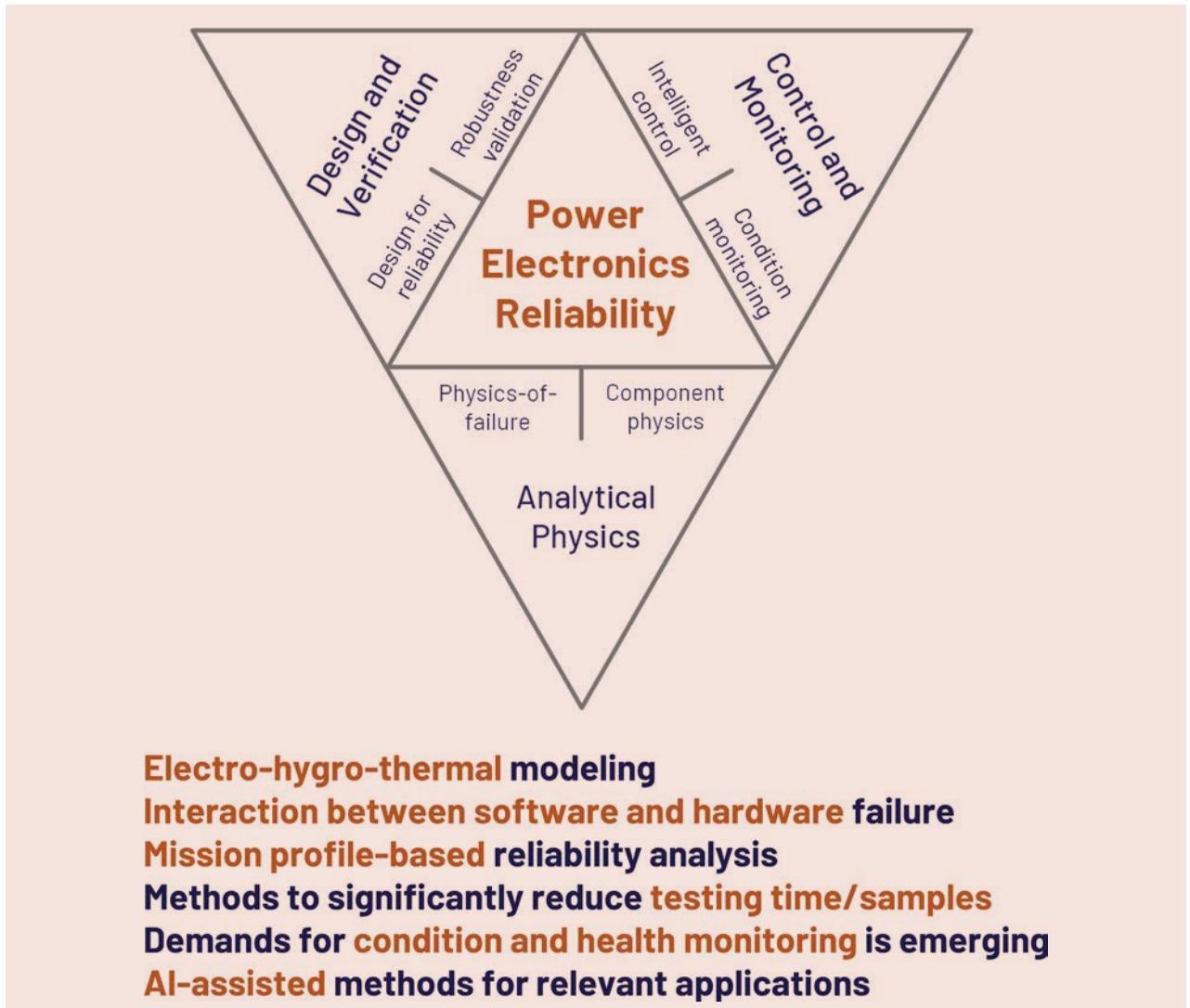


FIG 2 Three main research themes on power electronics reliability in the last ten years at Aalborg University and the research outlook. Source: Prof. Huai Wang, Aalborg University.

electronics-based power systems were considered as two of the most critical applications in the next decade regarding the degree of challenge to designers and reliability engineers [9], reliability requirements, and market size. Finally, the presentation called for efforts in education through Master/Ph.D. courses, open-access databases, and the technical community in this multi-disciplinary area.

The discussions and the presentations highlighted some future issues to be resolved or to get more attention in the next decade

- Early failures are still present in some renewable systems—means to avoid them are needed.
- Need for faster accelerated testing of components and systems combined with a better understanding of physics of failure.
- AI may be applied for faster accelerated testing and enable analysis to the end of life.
- Fusion prognostic approaches can be a powerful tool for end of life detection.
- Better physics of failure models for humidity/water and moisture impact.
- Validations of life-time calculation and predictions will increase thrust to modern reliability engineering analysis methods.
- Need for more research test infrastructure for battery/storage and power electronic components/converters including mission profile emulators to test for real applications.
- Better condition monitoring methods applying physics of failure models and eventually add physics informed neural network in the models (PINN).
- Initiatives should be formed for research available open access test data.
- Develop more educational programmes in this field.
- A technical committee working with these aspects could be formed in the IEEE Power Electronics Society.

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Need for faster accelerated testing of components and systems combined with a better understanding of physics of failure.

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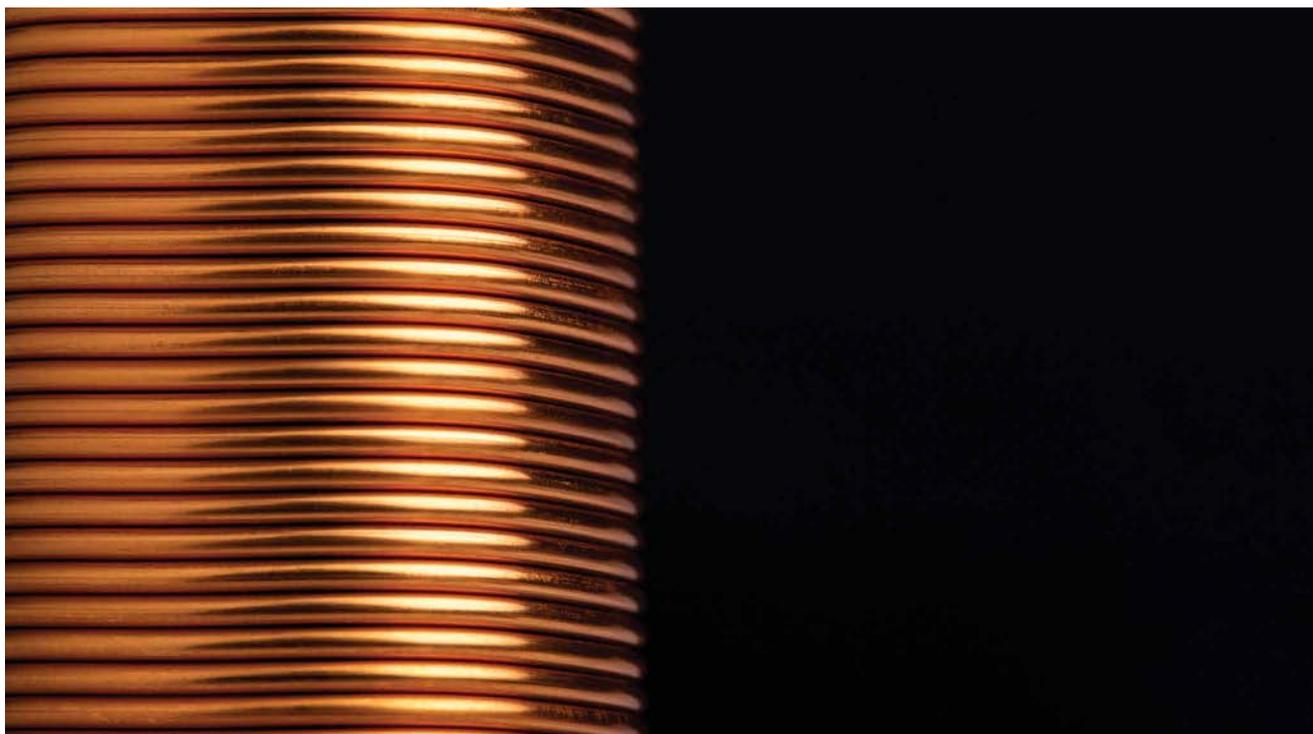
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Selecting the Best Magnetic Core Geometry

by Ira J. Pitel

Selecting the best core geometry for a given application can be challenging given all the options available. For high-frequency applications using ferrite and other low loss materials, many different shapes are available from core manufacturers. For power electronics applications, frequencies are not constrained to power line frequencies leading to more complex core designs. Proximity effects, nonlinear core excitation, and sensitivity to frequency are just some effects to consider for good designs. Whether designs are intended for 50 Hz or 100 kHz, the basic design equations are the same.

For those outside the field of magnetic design, the engineering for this technology is frequently regarded as a “black art” process. Getting good data for accurate modeling is difficult and often a heuristic design approach

is needed to optimize a magnetic design once all of the constraints are examined.

This article is intended to offer alternatives to available designs and known techniques, such as, interleaving primary and secondary windings of transformers and to present methods for reducing air gaps in inductors. The ideas presented here can be extremely effective with improving magnetic designs without increasing manufacturing costs. While there are many core shapes available, this article explores performance using nonstandard ratios of core cross-sectional area to winding window area.

The ideas presented here can be extremely effective with improving magnetic designs without increasing manufacturing costs.

Area Product

The first step in any magnetic design is to choose the magnetic core. This selection can be accomplished by multiplying the cross-sectional area of the core, A_e , with the cross-sectional area of the winding window, A_c [1]. Figure 1 illustrates a classical EI core design and equations (1) and (2) show the expressions for A_e and A_c . The product of these two terms is area squared—not volume—but the result is extremely useful to understanding design constraints. Other parameters of interest, that are common in the industry, are T for tongue, l_g , for air gap, l_m for magnetic path, and S for stack

$$A_e = T \times S \quad \text{in}^2 \quad (1)$$

$$A_c = W_W W_H \quad \text{in}^2 \quad (2)$$

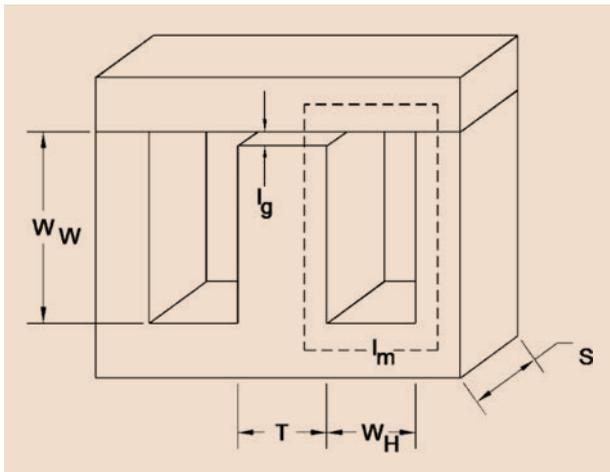


FIG 1 Magnetic core.

A_e , with sine wave excitation, is given as follows:

$$A_e = \frac{V_{\text{rms}} \times 10^8}{28.6 B_m N f K_1} \quad \text{in}^2 \quad (3)$$

where:

- V_{rms} : excitation voltage (V_{rms})
- B_m : maximum flux density (Gauss)
- N : number of turns
- f : excitation frequency (Hz)
- K_1 : stacking factor (percentage of magnetic material in core area. For a ferrite core, this number is 1.)

A_c , the winding window area, is given as follows:

$$A_c = \frac{.784 I_{\text{rms}} J N \times 10^{-6}}{K_2} \quad \text{in}^2 \quad (4)$$

where:

- J : current density (circular mil per ampere)
- K_2 : winding space factor (percentage of conductor in the window area. This constant is typically between 0.30 and 0.50 depending on the bobbin dimensions and insulating materials.)

Multiplying (3) by (4) yields the area product (5). The area product is a function of $V_{\text{rms}} I_{\text{rms}}$ which includes all windings of the transformer. The ratio of A_e to A_c is an independently controlled variable which has important effects on the core geometry and performance. Current density J is typically on the order of 300 CM/A for small bobbin type transformers and 1500 CM/A for multi-ton steel transformers

$$A_e A_c = \frac{2.74 V_{\text{rms}} I_{\text{rms}} J}{B_m f K_1 K_2} \quad \text{in}^4 \quad (5)$$

Like the area product for transformers, area product for inductors can also be determined by multiplying the cross-sectional area of the core, A_e , by the winding window, A_c . A_e in this case is given by equation (6) and the area product is represented by (7)

$$A_e = \frac{L I_{\text{max}}}{6.45 N B_m K_1 \times 10^{-8}} \quad \text{in}^2 \quad (6)$$

$$A_e A_c = \frac{12.16 L I_{\text{max}} I_{\text{rms}} J}{B_m K_1 K_2} \quad \text{in}^4 \quad (7)$$

where:

- L : inductance (Henries).

The interesting parameter of expression (7) is $L I_{\text{max}} I_{\text{rms}}$ which has a relationship to energy; this should be expected. Again, we have the ratio of A_e to A_c that is an independently controlled variable which has important effects on the core geometry and performance.

Winding Issues

As described in equations (5) and (7), the relative size is dependent on the product of A_e and A_c . Increasing A_e and decreasing A_c by the reciprocal does not change the size of the magnetic component. However, this geometric change has large effects on proximity effects, air gap length with inductor cores, wire ac resistance, core loss, leakage inductance, magnetizing inductance, and magnetic part efficiency. For steel cores made with laminations, stack adjustments are relatively common. For high-frequency cores; like those made with ferrite; double, multiple, and custom cores can have similar effects.

With a fixed winding window area, winding strategy has significant effects. To lower proximity effects—fewer turns yields better results. Interleaving primary and secondary windings, as illustrated in Figure 2, shows one method for lowering proximity effects. Interleaving can be done with both the primary and secondary windings for greater values of n , the number of dielectrics between windings.

Like increasing A_e and decreasing A_c , increasing n has similar results for reducing losses and driving down the temperature rise. Other ameliorative measures include increasing the length of the coil, W_w , in relations to the height of the coil, W_H . Using U-U cores with two coils has similar effects as interleaving with one coil. Both techniques have positive effects on reducing leakage inductance.

To illustrate some of these points, an experimental test transformer is presented having different ratios of A_e to A_c along with interleaved windings. The transformer is defined as follows:

- Primary Voltage, Current: 250 V, 3.0 A
- Secondary Voltage, Current: 125 V, 6.0 A
- Primary Wire: 4 strands #25
- Secondary Wire: 8 strands #25

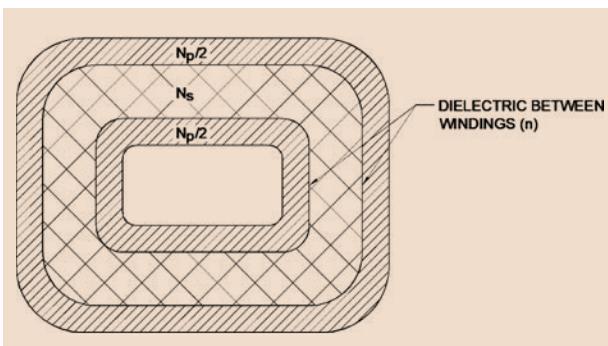


FIG 2 Coil with sandwiched windings. (Viewed from top of coil. $N_p/2$ is the primary turns and N_s is the secondary turns.)

Turns: see Table 1

Flux Density: 2.275 kG

Excitation Frequency: 25 kHz

With a standard E21 core geometry, changing the winding structure from transformer A to B (sandwiched), drops the wire losses from 3.69 to 2.72 W. Transformer C shows further improvement can be made by using a commonly used winding arrangement, as illustrated in Figure 3, by doubling A_e and reducing the winding window A_c in half. While the mean length turn and core loss increases, winding loss decreases. This result is caused by lower wire resistance. With a double stacked core and applying sandwiching, transformer D, additional reduction in losses can be achieved.

Finally, a stack of four cores continues to reduce winding losses, but core losses negate any improvement.

Air Gaps

For designing inductors, it is common practice to place air gaps in the magnetic path to reduce the effective permeability. There are some core materials, like Kool Mu, a product from Magnetics, that have air gaps built into the core material, however in general, high-permeability material requires air gapping to reduce the permeability for power inductor applications. A large air gap produces a fringing field that can penetrate the coil causing localized heating. A good thumb rule for defining an acceptable air gap is to keep the spacing between the core and coil greater than the air gap. If the bobbin thickness satisfies this requirement, then localized heating around the air gap is minimized. One method to reduce fringing field is to place multiple gaps which can be achieved using an E core with one gap in the center and the other gap in the outside legs. Adding more gaps, while doable, can be a mechanical challenge.

Equation (8) shows the relationship of an air gap to turns. Decreasing turns reduces air gap requirements. Increasing the ratio of A_e to A_c can be used to lower air gap requirements and thus improving the negative effects of fringing fields

$$l_g = \frac{.495NI_{\max}}{B_m} \quad \text{in} \quad (8)$$

Like the transformer example in Table 1, an experimental inductor is presented with different methods of air gap placement in Table 2.

Primary Voltage, Current: 270 V, 2.64 A

L: 0.65 mH

Wire: 4 strands #25

Turns: see Table 2

With a fixed winding window area, winding strategy has significant effects.

Table 1. Test transformer parameters.

Transformer	N_p	N_s	n	$A_e^{(1)}$ (in ²)	$A_c^{(1)}$ (in ²)	Core Loss (W)	Wire Loss (W)	Mean Length Turn (in)	Trise (°C)
A	32	16	1	0.240	0.264	1.23	3.69	0.246	95.7
B	16+16	16	2	0.240	0.264	1.23	2.72	0.246	76.9
C	16	8	1	0.480	0.132	2.45	1.17	0.328	58.7
D	8+8	8	2	0.480	0.132	2.45	1.01	0.328	56.1
E	8	4	1	0.960	0.066	4.91	0.64	0.491	63.6

Note (1):

Core A, B: standard E21

Core C, D: double stacked E21 with A_c reduced in half

Core E: quadruple stacked E21 with A_c reduced to a fourth

A_e : is the cross-sectional area of all cores combined

A_c : Cores C, D, and E were modified to have a reduced E21 window

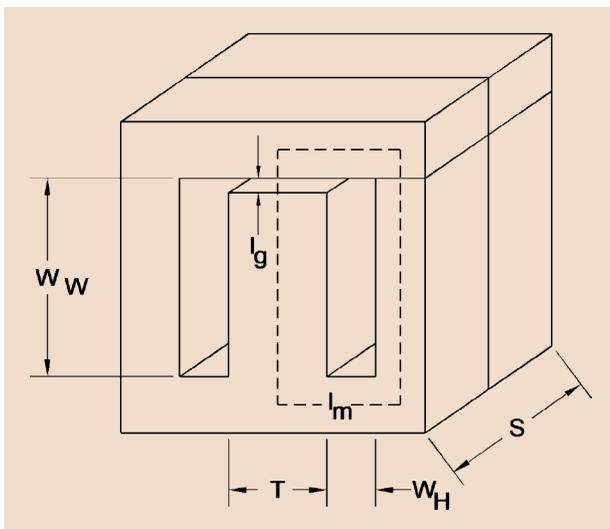


FIG 3 Double stacked core with half A_c .

Flux Density: 2.45 kG

Excitation Frequency: 25 kHz

With a fully utilized bobbin in inductor A, eight layers of winding are needed driving up proximity losses and producing 8.85 W of wire loss. Doubling the core and reducing the winding window, A_c , by a half reduces wire losses to 1.91 W in inductor B. Also, the center leg air gap requirement drop from 0.139" to 0.041". Considering the bobbin thickness, a 0.041" air gap would produce a reasonable fringing field. Placing air gaps in both the center leg and outside legs, 2 breaks, would further reduce the fringing fields as illustrated in inductor C. The air gap for inductor C is 0.008" in the center leg

and 0.008" in the outer legs. Note that adjustments have been made to compensate for the fringing fields. Using four cores, as shown for inductor D, has further positive effects.

Examples

One powerful benefit of adjusting the ratio of A_e to A_c is the ability to place the magnetic part in unusual enclosures. A good example is the 1 U, 1.75" enclosure used for a standard power supply manufactured by Magna-Power Electronics.

With this height limitation, further design parameters must be considered, such as top and bottom covers, insulation, clearance allowance between cabinets, and brackets to hold down magnetic parts. For the 1 U enclosure discussed here, these numbers reduce the allowable height of the magnetic part from 1.75" to approximately 1.40". Figure 4 illustrates three magnetic parts designed to fit within a 1.40" height requirement: a 10 kW transformer, chopper choke, and input choke. None of these designs would meet the height requirements unless the ratio of A_e to A_c were adjusted above the ratio normally used for an open frame, stand-alone magnetic component.

To illustrate the effectiveness of this strategy, an input choke was designed in two ways: a typical ratio of A_e to A_c and another with a core designed to fit in this particular application. A core with a typical A_e to A_c ratio uses standard 100EI laminations and one with a non-typical ratio uses 21EI laminations. Table 3 highlights the physical core design and Table 4 shows the design results. Results for the design are similar, except that the height for the core

One powerful benefit of adjusting the ratio of A_e to A_c is the ability to place the magnetic part in unusual enclosures.

Table 2. Experimental inductor.

Inductor	N	Total Number of Air Gaps in the Core	$A_e^{(1)}$ (in ²)	$A_c^{(1)}$ (in ²)	Core Loss (W)	Wire Loss (W)	Total Air Gap	Mean Length Turn (in)	Trise (°C)
A	64	1	0.240	0.264	1.23	8.85	0.139	0.246	196.4
B	32	1	0.480	0.132	2.45	1.91	0.041	0.328	70.6
C	32	2	0.480	0.132	2.45	1.91	0.016	0.328	70.6
D	16	1	0.960	.066	4.91	0.68	0.015	0.491	64.1

Note (1):

Core A: standard E21

Core B, C: double stacked E21 with A_c reduced in half

Core D: quadruple stacked E21 with A_c reduced to a fourth



FIG 4 10 kW transformer, input choke, and chopper choke.

with 100 EI laminations is 2.54" and the one using 21EI laminations is 1.33".

Figure 5 shows the coil, core, and assembly of the input choke manufactured with 21EI laminations. There is nothing particularly unique assembling this part other than its large stack. As for the other two parts in Figure 4, the chopper choke is designed to operate at 41 kHz. A steel core cannot be used here. To meet the requirements, a K4317-E060 Kool Mu core manufactured by Magnetics was chosen. Again, we have the same height constraints as before, so the selected core has a similar height as the 21EI steel lamination. To meet the inductance requirements, five cores were stacked together. As illustrated, custom bobbins were manufactured and tooled for the input and chopper chokes.

Mounting the two chokes to the chassis allows both conduction cooling at the bottom of the core and air cooling within the enclosure. The transformer must fit within the height of the enclosure and as observed from Figure 4, it is mounted horizontally. Used in a hard switched circuit topology, adds a secondary requirement of very, low leakage impedance.

The core is fabricated with four, I93/28/16 ferrite cores, dimensions are 0.630" × 1.083" × 3.666" each. The ends of two cores are trimmed to 3.590" and the other

Table 3. Core parameters.

Core	N	AWG	S (in)	W_w+T (in)	A_e (in ²)	A_c (in ²)	Air Gap	Total Number of Air Gaps in the Core
100EI	35	.144x.072	1.15	2.54	1.15	0.75	0.041	2
21EI	15	.128x.064	5.00	1.33	2.50	0.25	0.016	2

Note:

Height: W_w+T

Table 4. Design parameters.

Core	L (mH)	I_{dc} (A)	B_m (kG)	Mean Length Turn (in)	Core Loss (W)	Wire Loss (W)	Core (LB)	Wire (LB)
100EI	0.65	38	13.6	0.489	1.81	18.5	1.81	0.63
21EI	0.65	38	13.3	0.998	2.19	22.5	2.09	0.47

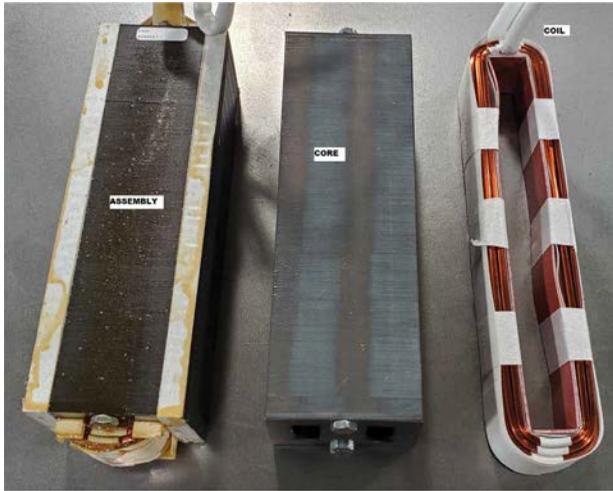


FIG 5 Input choke assembly, core, and coil.

two cores are cut to 3.035". The four cores are glued together giving a thickness of 0.630" when assembled. Mounting the transformer in a horizontal position, using double coils to reduce proximity effects, and using a long winding width, W_w , allow placement of the transformer in the enclosure and provide a low leakage impedance. Removing heat by a conductive path is not possible here. Strong air flow is required and the transformer needs to be placed near cooling vents. An internal heat sink, illustrated by the circular copper fabrication, improves losses on the bottom layer of the coils and the coil insulation over the finished coils are purposely removed to have better cooling on the top layer.

Conclusion

Magnetic core geometries have significant effects on the performance of transformers and inductors. Reducing turns and increasing the cross-sectional core area, A_e , can be accomplished without increasing the size of the magnetic component. As illustrated in this article, the area product, $A_e A_c$, is the parameter defined to keep constant; this allows A_e to be increased as A_c to be decreased. Using this parameter, proximity effects can be optimized.

Results are similar to applying sandwiching techniques to the windings.

Adjustments to the area products can be achieved by using a smaller core and stacking a quantity of them together. Special bobbins, which have proper dimensional characteristics, are readily available. Cosmo is one source that offers such bobbins. For larger high-frequency magnetic cores, piecing magnetic blocks together offers still more options to obtaining a custom core.

Magnetic cores with greater A_e to A_c ratios tend to yield better magnetic designs. This recommendation is put forth to magnetic core manufacturers in hopes that more core choices will become available with higher A_e to A_c ratios than are currently being offered. In the meantime, work around measures include stacking standard cores and/or building custom cores with magnetic blocks.

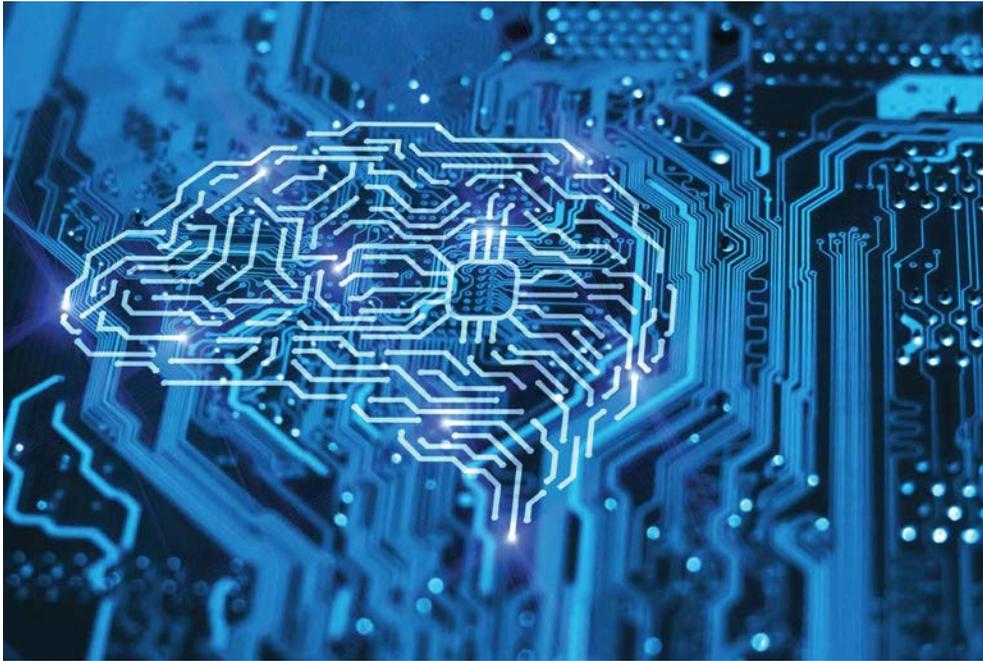
About the Author

Ira J. Pitel (ipitel@magna-power.com) received the B.S. degree from the State University of New Jersey at Rutgers in 1972, the M.S. degree from Bucknell University in 1975, and the Ph.D. degree from Carnegie-Mellon University in 1978. In 1981, he founded Magna-Power Electronics, a company specializing in custom and standard power conditioning products. He is responsible for technology oversight of its line of 1.5–3,000+ kW ac–dc power supplies. In 1986, he joined Texas A&M University as an Adjunct Professor. He holds 29 patents in the field of power electronics. He was a co-recipient of the Society Prize Paper Award of the IEEE Industry Applications Society (IAS) in 1995. He was honored as the Rutgers Outstanding Engineering Alumnus in 2000 and the Gerald Kliman Innovator Award in 2008. He is a Life Fellow of the IEEE and has served in many IEEE capacities including society president of the IAS. He is a member of the Eta Kappa Nu and Tau Beta Pi.

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Machine-Learning-Based Condition Monitoring of Power Electronics Modules in Modern Electric Drives

by Dinan Li, Panagiotis Kakosimos, and Luca Peretti

Integrating machine-learning (ML) models responsible for predicting the evolution of those directly collected or implicitly derived parameters enhances the smartness of industrial systems even further. In this article, data already residing in most modern electric drives has been used to establish a data-driven thermal model of power electronics modules. The

developed method relies solely on existing information in the electric drive enabling its wide applicability. Adding more sensors to a product is a complicated task, thus it is not a desirable solution. For training and validating the thermal digital twin, a test bench has been designed specifically. Several approaches, from traditional linear models to deep neural networks, have been implemented to emanate the best ML model for estimating the case temperature of the module. Numerous evaluation metrics were then used to assess the investigated methods' performance and implementation in industrial embedded systems. The proposed solution performed satisfactorily while the powertrain underwent various static and dynamic operating profiles. The model identified a blockage in the air outlet of the drive by monitoring the deviation of the measured and estimated temperatures, thus it prevented the power module from experiencing a fatal failure.

Introduction

Today, an industrial drive is much more than a device that produces the necessary output signals to adjust the motor speed and torque; it constitutes the core of the powertrain. An electric powertrain may comprise several components, including the drive, motor, energy storage, and mechanical transmission system (Figure 1). Measured signals for controlling an asset usually contain insightful information about not only the specific asset but also the rest powertrain components and even the application. Therefore, a drive gathers plenty of information about a system's operation, making it feasible to identify and eliminate possible limiting factors and optimize the whole

powertrain's performance. A simple yet effective example is a drive used to reduce the occurrence of pump cavitation. In the context of modern and connected industrial systems, drives play an even more vital role by being equipped with several sensors and powerful microprocessors. The physical assets may be surrounded by several IoT peripherals that link to cloud services or support the execution of artificial intelligence (AI) algorithms on the edge [1]. The possibility of utilizing the vast amount of data residing in an electric drive and processing them locally or remotely opens new prospects in industrial digitalization [2].

Monitoring the thermal behavior of an asset by estimating its temperature under various operating scenarios has been among the major applications of ML/AI [3]. Today, ML models offer unmatched performance over classic thermal modeling approaches without requiring sophisticated hardware architectures and enormous resources [4]. Temperature signals, previously utilized as threshold limits under heavy-duty conditions in industrial systems, can now be used to monitor and optimize performance under any operating condition. Temperature ratings of powertrain components can benefit by retrofitting the thermal model output to design and dimensioning tools [5]. Under faulty conditions, the thermal digital twin may inherently attempt to forecast the device temperature; however, proper adaptations may support the detection of deviations from the expected trajectory and signal an alert [6].

It is thus evident that estimating or forecasting the temperature of an asset is crucial for energy saving,

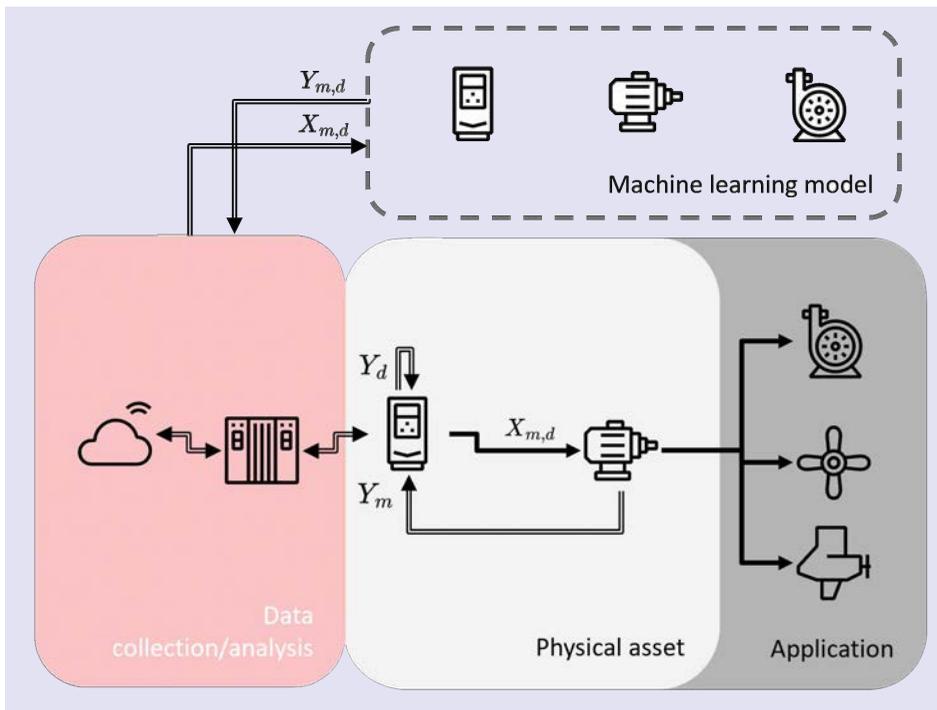


FIG 1 Block diagram of a modern electric powertrain.

performance optimization, condition monitoring, and lifetime extension, among others [7], [8], [9]. Establishing the relationship between electric power losses and temperature variation has been studied and led to the development of advanced analytical or computational thermal models [10]. However, precise knowledge of the electric power losses for estimating changes in thermal behavior is necessary. Identifying the losses during the system operation while several unexpected factors influence its behavior is a challenging and sometimes unsolved task [11]. Therefore, static thermal models under known operating conditions are usually employed in the end. In order to overcome this issue, all factors that impact thermal behavior must be used in a model that tracks real-time temperature changes utilizing a formed relationship between measured signals and temperatures [12].

An ML model can be used to establish this relationship by understanding how already measured input parameters, X , are correlated with output temperature signals, Y , for the power converter, d , or even the motor, m (Figure 1). Adding more layers to a neural network structure may further assist in considering even more abstract phenomena without explicitly defining their interactions with the temperature.

This article explores the utilization of existing measured signals in today's electric drives to estimate the case temperature of power electronics modules operating under static and dynamic conditions. An accurate loss estimation is not required because the ML model can account for their impact on the temperature variation directly from the measured signals. The case temperature of a power electronics module has been used as an illustrative example; nevertheless, similar results and conclusions can be drawn for estimating the thermal behavior of electric motors or any other powertrain component.

Specifications of the Machine-Learning Model

The development of any ML model requires the utilization of a pipeline that assembles several steps and cross-validates them together by setting different parameters (Figure 2). The first step of such a pipeline is the data collection and preparation for training the ML model. The main goal is to develop a data-driven thermal model of a power electronics module, so the drive must undergo several tests where speed and

load conditions are varied. For this purpose, seventeen profiles of about eight hours each with both fast and slow dynamics have been created. The specifications of the investigated electric powertrain have been summarized in Table 1 where the considered converter topology is that of the classical two-level dc-ac voltage source converter.

During the execution of each profile, several internal drive parameters have been captured with a sampling frequency of about 1 Hz, through a low-rate interface usually available to customers. At this point, the cross-validation of all the captured parameters dictates the ones that must be added to the model because they influence the power module temperature. The selected parameters (Table 2) are directly related to the temperature changes, whereas the ambient temperature is needed to provide the environmental conditions.

More specifically, in electric drives, the power electronics module is the main heat source due to the conduction and switching losses. The drive current and output power, which have been selected as model inputs, are clearly associated with the conduction losses. The switching frequency, which affects the switching losses, is not among

Table 1. Specifications of the investigated setup.

Motors	Test motor
Type	Induction machine
Power rating	15 kW
Voltage rating	400 V
Current rating	30.6 A
Torque rating	97 N m
Pole pair number	2
Nominal speed	1478 rpm
Cooling means	Attached fan blades
Drives	Test drive
Type	ACS880-01-038A
Topology	2-level, IGBT
Power rating	26 kVA
Current rating	38 A
Cooling means	Forced air

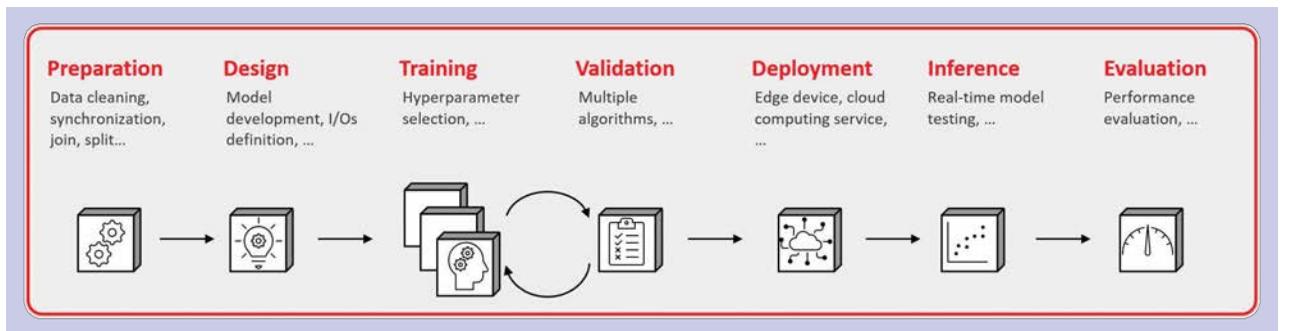


FIG 2 Process of model development.

the selected parameters because it remained constant during the system operation. The heat dissipation to the environment is achieved through the thermal material interface, heat sink, and fan. Therefore, a possible temperature increase may be attributed to any of the mentioned heat injection and dissipation mechanisms. In addition to those parameters, feature expansion has also been conducted by adding eight exponentially weighted moving averages for considering the past thermal behavior.

In the next step, various ML models of different complexity have been tested, and their performances in estimating the case temperature have been evaluated by splitting the datasets for testing, training, and validation. In machine learning, a loss or cost function is a function that is used to represent how well a model fits the data. The loss function is computed given the model's estimation and the measured real value. There are many candidates for loss functions, and they can be classified based on the nature of the targets. Since data collected from the field is necessary for training the ML model here, only supervised ML algorithms taking continuous target variables have been investigated. Several models have been benchmarked before selecting the most appropriate ones (Figure 3). The following ML models are among the most prevalent for similar applications by being superior in terms of complexity and hardware resources:

- **Linear regression (Elastic Net)** is the simplest approach to be considered. This model assumes the presence of a linear correlation between the scalar response and one or more explanatory variables. Regularization may be utilized to penalize the terms of the employed loss function, thus preventing overfitting, and improving the model's generalizability.
- **A multilayer perceptron (MLP)**, or fully connected neural network, is the most straightforward feed-forward network. It often includes three main layers: an input layer, a hidden layer, and an output layer consisting

Table 2. ML model inputs and target outputs.	
Parameter	Symbol
Measured inputs	
Output frequency	f_d
Output current	I_d
Output power	P_d
Ambient temperature	T_{amb}
Target outputs	
Case temperature	T_c

of many neurons. The neurons between two consecutive layers are interconnected to render a fully connected neural network. The values of subsequent neurons are calculated as a linear combination of the previously connected ones by applying an activation function.

- **Convolutional neural networks (CNNs)** are most commonly applied to image processing because of their capacity to explore spatial data; however, the one-dimensional variant constitutes a great fit to analyze temporal data. Unlike a fully connected network, data must come sequentially for a temporal CNN to work. Each neuron has information from not only the current time step but also from previous inputs. When more convolutional layers are assembled, neurons at the last layers can instantly get information from inputs that were derived in the past layers.

A critical step of the ML model development is tuning the hyperparameters. Some parts of the process can be fully automated using Bayesian optimization; however, other parts require careful consideration of the model behavior, thus consuming significant time and computational resources. Model validation is also a rigorous and

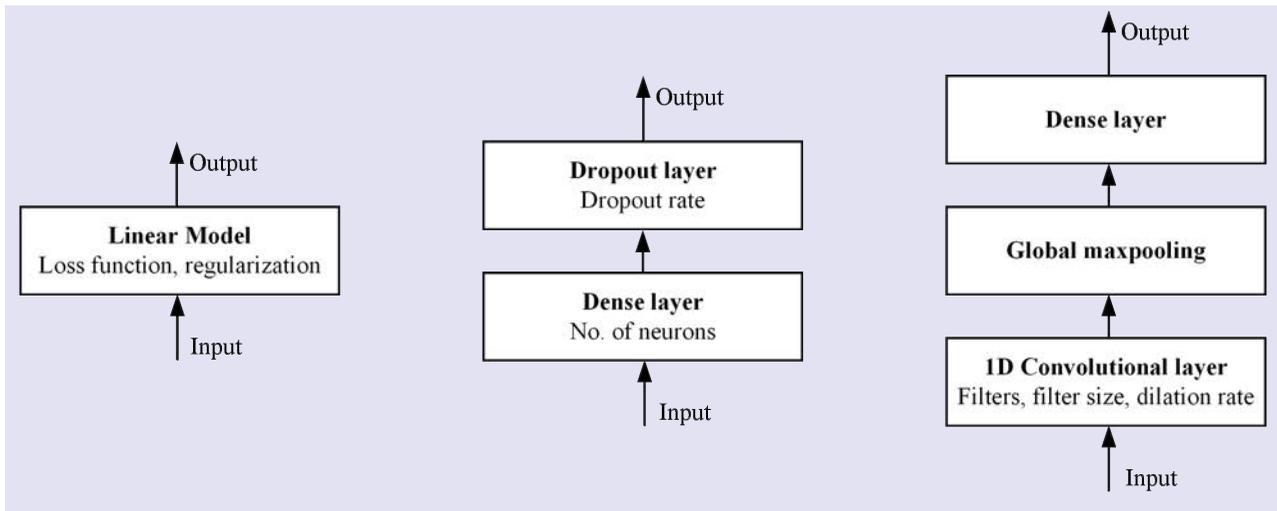


FIG 3 Block diagrams of Elastic Net, MLP, and CNNs, from left to right.

scholastic step. All the generated profiles have been used to train the model and compare its behavioral changes to enhance the performance even further. After finalizing the model structure and configuration, it can be deployed to an edge device or a cloud computing service. The role of the edge device can be served by the same electric drive or gateway in a modern electric powertrain (Figure 1). Once the model has been designed and deployed, it is possible to use it for obtaining estimations of the case temperature by running inference. At this final point, the model can be further adjusted by running performance tests and considering several evaluation metrics.

Operating Cycles of the Electric Drive

Various static and dynamic input profiles have been used to produce the needed training datasets by feeding the frequency (or speed) and applying load torque to the test drive and motor, respectively (Table 1). Usually, repeating cycles are performed in several applications; however, different scenarios have been tested in this article to explore the model's capability and performance limits. All the generated frequency and load profiles have been used to train

the ML model; however, some profiles have been kept separate to further validate its performance. One of these profiles is shown in Figure 4, where the system initially starts from thermal equilibrium, followed by a period of constant output frequency and motor load. Then, the operation becomes more dynamic with sudden changes in both frequency and load. Under these circumstances, the irregularity of the operation makes temperature monitoring even more challenging for an ML algorithm.

Since the electric drive controls the speed of a motor, its current must remain within its operating limits. As shown in Figure 5, the current stays below its nominal value, although overloading the motor is likely under certain conditions. Another significant input parameter is the ambient temperature, as the model needs to know in which environmental conditions the system is operating. The ambient temperature is typically measured with sensors located in external locations of the electric drive or close to its fan. In the conducted tests, the temperature did not vary drastically; however, there are cases where enclosed systems suffer from inadequate cooling, making temperature inclusion a prerequisite for precise temperature estimation.

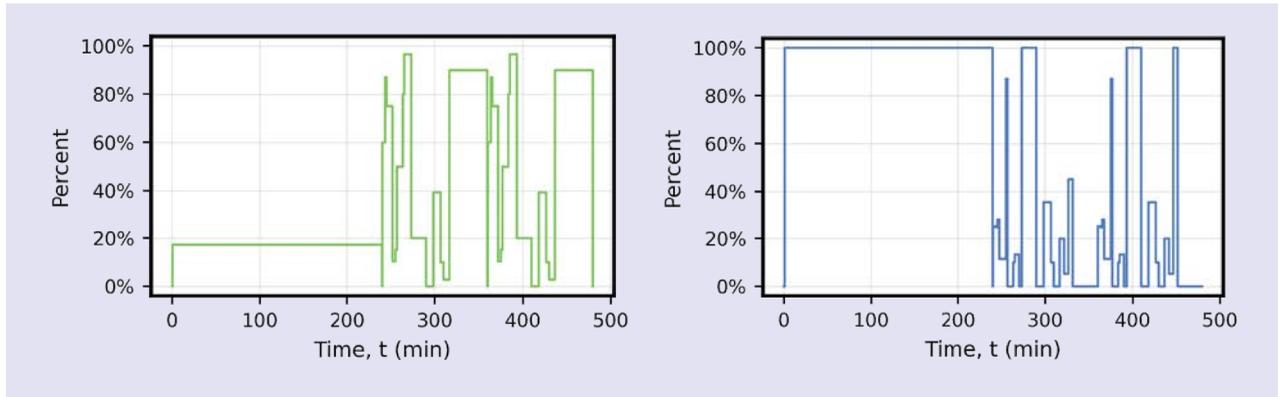


FIG 4 Normalized output frequency (left) and load (right) profiles.

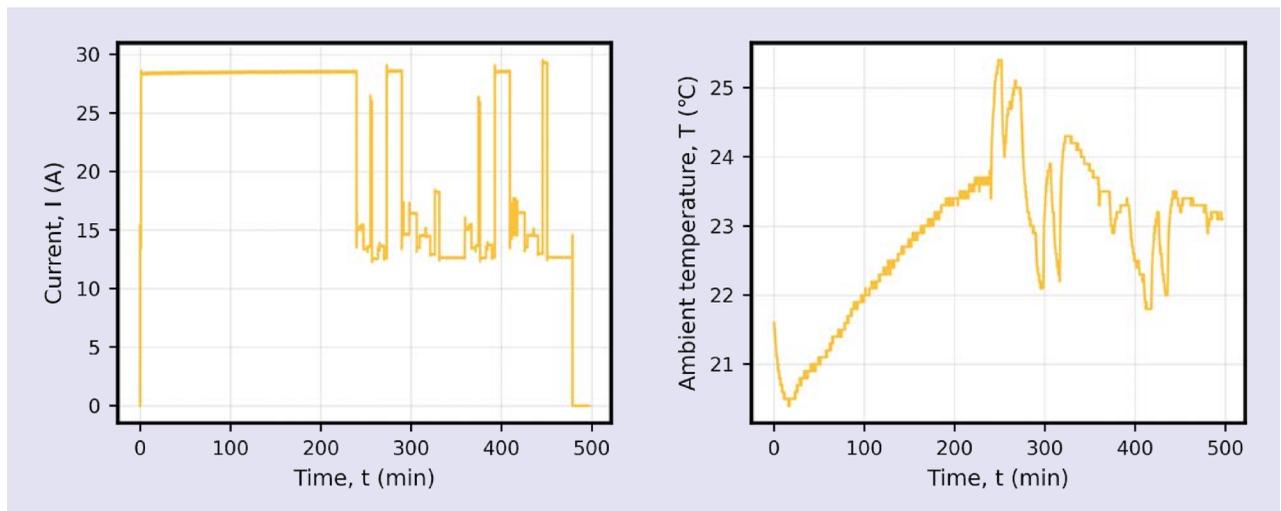


FIG 5 Motor current and ambient temperature.

Estimating the Power Electronics Module Temperature

The trained ML model has been used to estimate the case temperature of the power electronics module after performing the operating cycle in Figure 4. It is worth highlighting that the selected profile was not the best-performing one; nevertheless, it has been selected to emphasize both the model performance and complexity. More specifically, the

results of the three developed models have been summarized in Figure 6. All the models perform satisfactorily and maintain an error within the range of $\pm 8\text{ }^{\circ}\text{C}$ even under highly dynamic conditions. Deviations at the beginning of the operation are attributed to the initialization of the expanded features of the moving averages. In the second half of the operation, there is also a good agreement between all the measured and predicted temperatures.

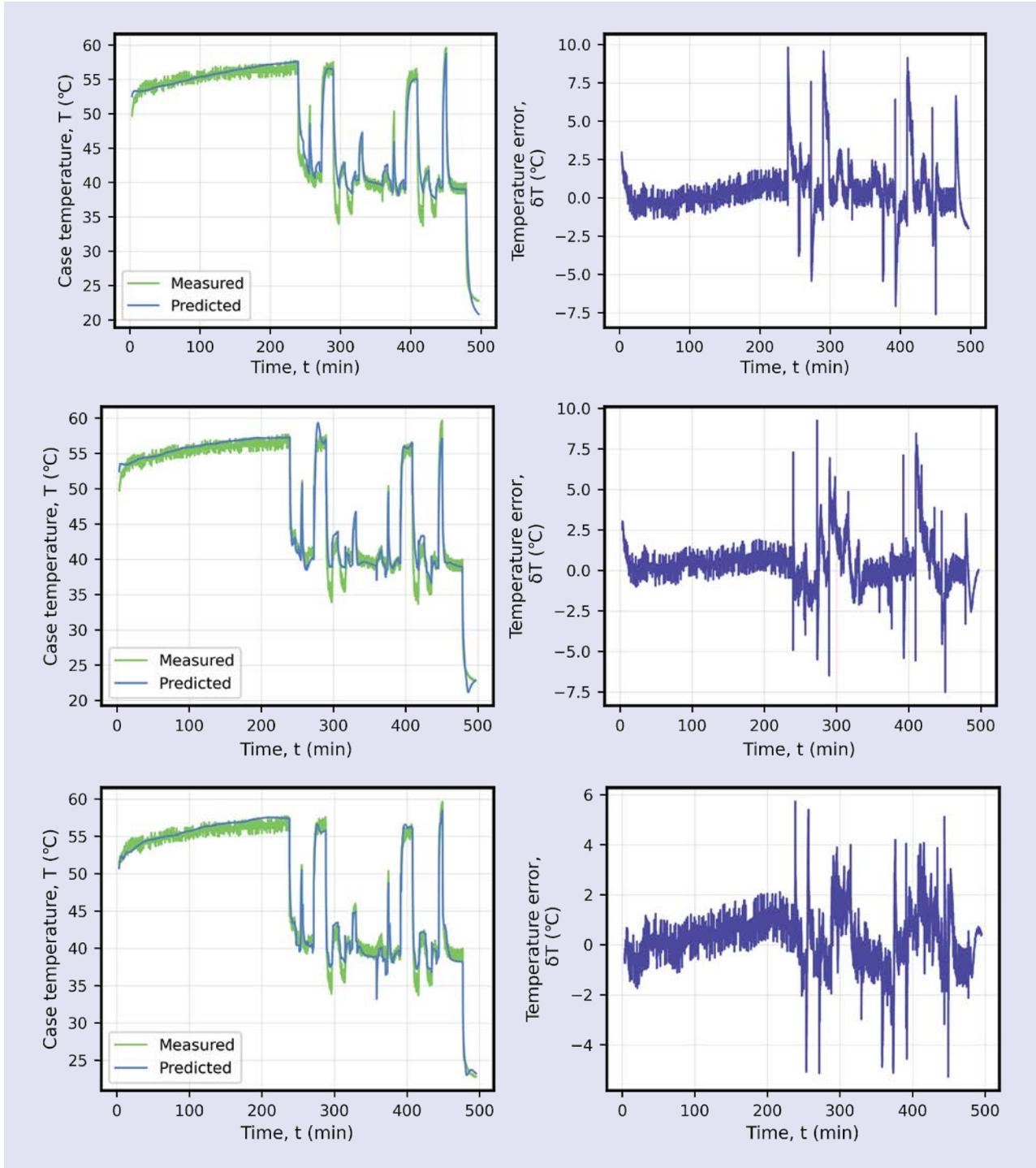


FIG 6 Estimated and measured case temperature with Elastic Net, MLP, and CNNs, from top to bottom. The temperature error is shown in the second column.

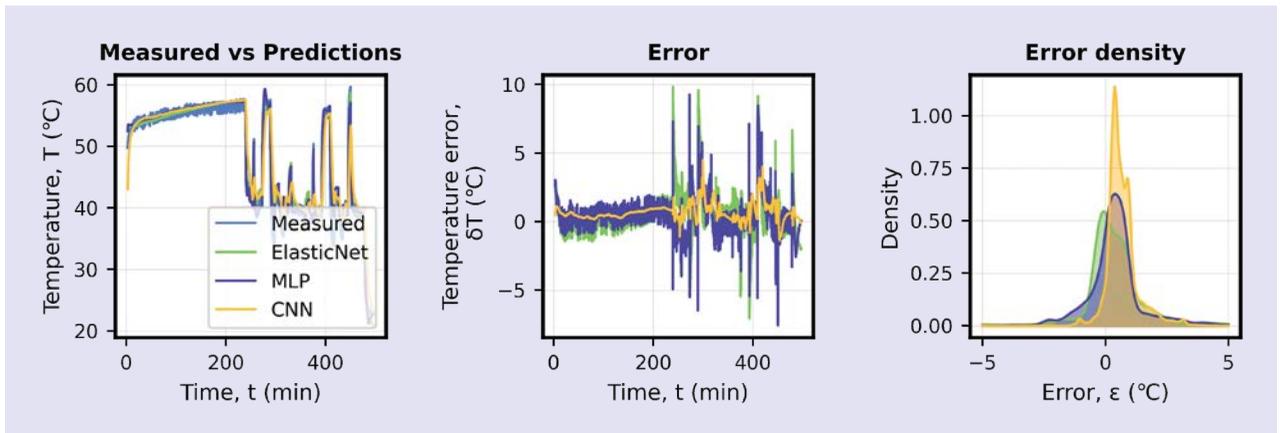


FIG 7 Measurement versus predictions, temperature error, and error density.

The comparative analysis of all the methods has shown that CNNs achieved minimal error during the whole power cycle (Figure 7). MLP succeeded in keeping the error stretched over the area around zero, whereas linear regression with Elastic Net was more biased by exhibiting larger errors during transients. Nevertheless, if the focus was on the first half of the operation after the moving averages have been initialized, then all models were more effective. In several applications, a temperature error within 10 °C is considered exceptional for any model. Considering also that the tested operating cycle has been highly dynamic, it can be safely concluded that all the investigated models have successfully estimated the case temperature.

In addition to the visual assessment of the performance, several metrics have been used to evaluate the different approaches. Instead of relying on a single profile and concluding that an ML model may not be sufficient, all seventeen profiles have been tested by retraining the ML model and excluding the investigated profile each time. All the results have been summarized in Table 3. In this case, CNNs exhibited the lowest mean squared error (MSE) and mean absolute error (MAE), whereas the other two models, Elastic Net and MLP, also performed adequately. In terms of complexity, the linear model needed the minimum number of parameters with training and inference times of ~9 times and ~500 times faster than

CNNs. Based on the application needs and computational capabilities of the edge device, the most suitable method must be selected.

Furthermore, it is interesting to investigate which parameters and their features were the most impactful on the temperature estimation accuracy. A correlation matrix has been employed to select the used parameter subset by visualizing hidden patterns; however, at a later stage, the selected parameters have been expanded with more features. For explaining the individual model predictions, the SHAP method is employed by calculating the contribution of each feature separately (Figure 8) [13]. As expected, the motor current and its moving average of a 3-minute span were the most impactful. The output power and ambient temperature also played a critical role. All these parameters are directly related to the electric power losses of the drive and its boundary conditions with the environment; therefore, it is evident that their impact should be high. The same consideration cannot be applied to the expanded features, though, because the effect of the historical drive operation cannot be easily implied heuristically.

Condition Monitoring: A Case Study

Estimating internal drive temperatures with this high accuracy level is extremely valuable, especially if

Table 3. Summary of the evaluation metrics under all the tested profiles.

Model	MSE	MAE	R^2	I_{∞}	Training time (s)	Inference time (s)	Parameters
ElasticNet	2.33	1.05	0.92	10.45	4.61	0.005	72
MLP	2.63	1.07	0.92	8.53	49.55	0.95	8k
CNN	0.94	0.68	0.96	3.74	403.84	2.46	6k

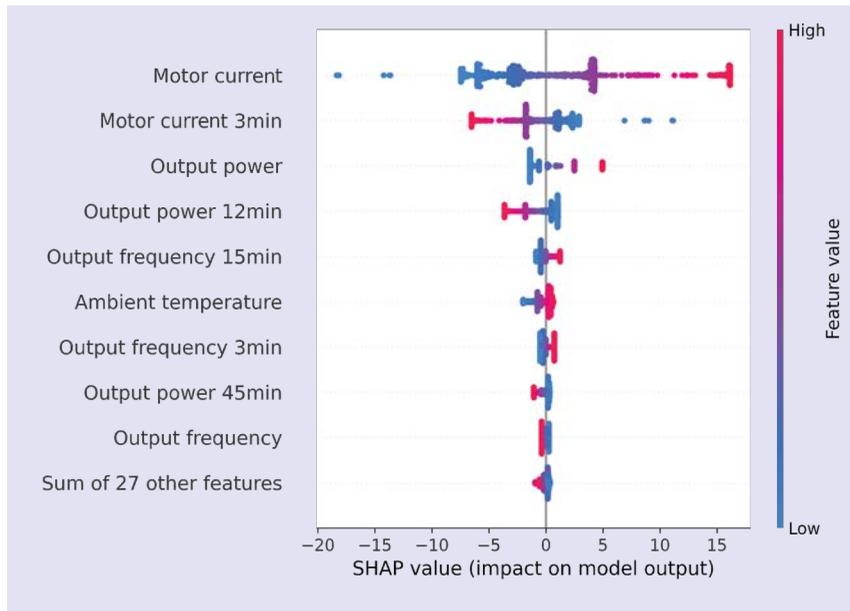


FIG 8 Impact of the parameters on the model output.

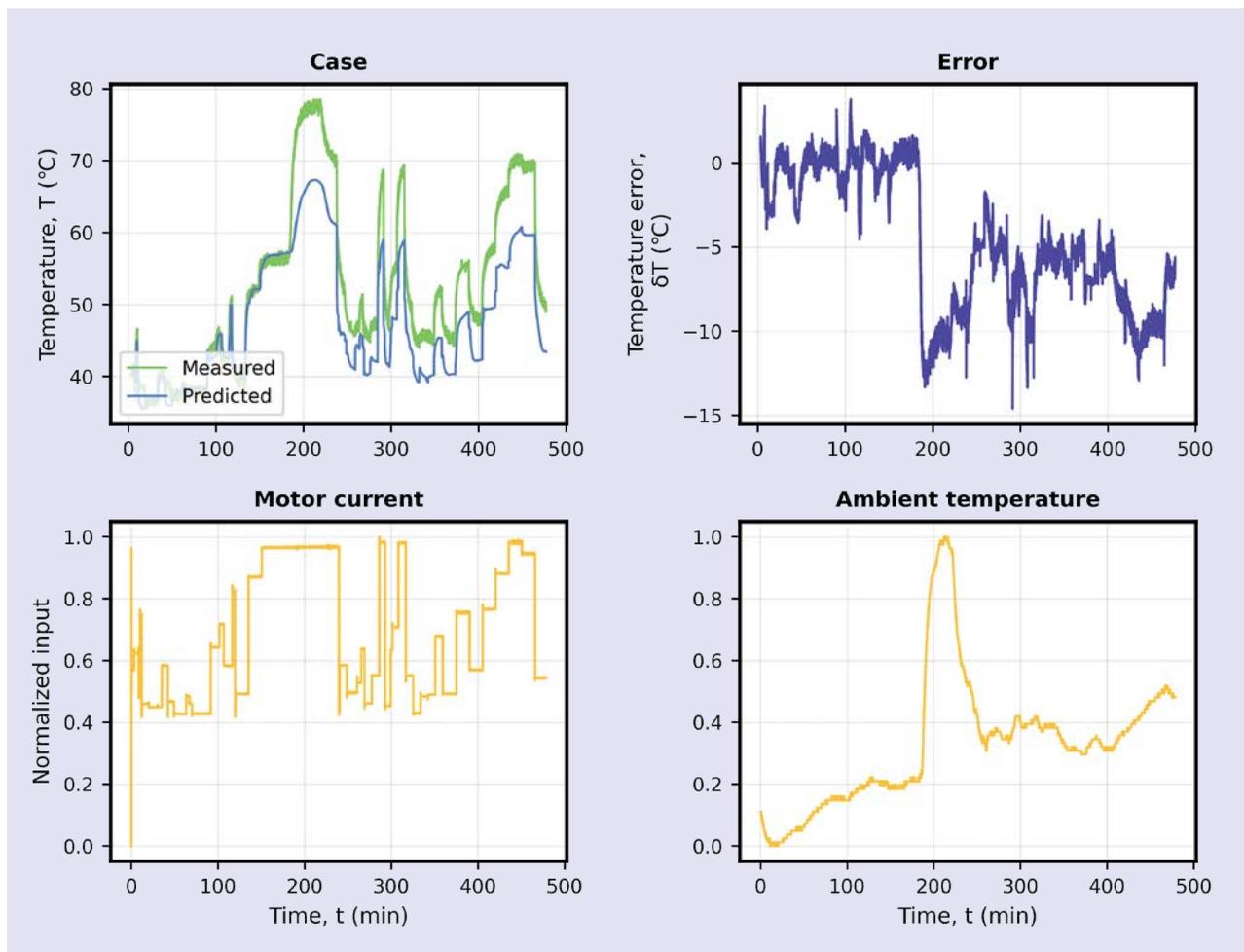


FIG 9 Model performance with partially blocked air outlet after about 3 hours of operation.

additional sensors are not needed. One of the primary use cases of temperature utilization is condition monitoring. The ML model can provide the anticipated temperature based on past system performance. A comparison with measured data from the field can potentially reveal significant findings about its current condition.

For the sake of demonstration, since forced air is used to cool the investigated drive, the air outlet has been partially blocked on purpose after 3 hours of operation in a new operating cycle unknown to the ML model (Figure 9). The error between the measured and predicted temperatures becomes large at the moment of the blockage and remains large for the rest of the cycle.

This demonstration is of practical use because industrial systems usually suffer from high temperatures due to dust buildup on the fins or around the vents. The variation of the temperature error can warn about the harsh operating conditions, thus preventing a fatal failure from occurring in the first place. A particular remark here is that the introduced failure also impacts the predicted temperature. This behavior is attributed to the fact that the ambient temperature used as a model input is measured at a location close to the air outlet, thus being impacted by the fin blockage.

Summary

Industry digitalization has significantly brought powerful embedded systems into the spotlight, changing almost every traditional aspect of power plant operation. Training and running ML models on edge is now feasible, bringing promising results. This article demonstrated a data-driven thermal model that used information already residing in most modern electric drives and predicted the case temperature of a power electronics module. Conventional linear models (Elastic Net) and deep neural networks (MLP, CNNs) have been investigated for temperature estimation under static and dynamic operating profiles. All models performed satisfactorily but exhibited different characteristics. A compromise based on the application must be made for selecting the simplest algorithms against the most computationally intensive but accurate ones.

The condition monitoring of electric drives and every other industrial system is about to change drastically due to the high effectiveness of ML in detecting abnormalities. Human intervention may remain high in the coming years, but as ML becomes more confident by the accumulation of more data, there will be more increased machine independence in the decision-making process.

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Celebrating the Tenth Anniversary of IEEE PELS WIE Committee

It's the 10th anniversary of the IEEE Power Electronics Society (PELS) Women in Engineering (WIE) Committee, and we've come a long way! In this article, we'll cover highlights from the past ten years, which includes recent achievements, our updated mission statement, and a look forward to some exciting planned activities. Some of those future plans include monitoring progress from a newly implemented data-driven approach to improving diversity across all facets for PELS members, supporting our members' career development both in-person and through a diverse offering of virtual events, and the outreach we're working on with PELS, the rest of IEEE, and beyond.

The PELS WIE Steering Committee was formed in 2013 under the leadership of Dr. Maryam Saeedifard to support PELS' commitment to inclusiveness and diversity. PELS (and the IEEE as a whole) is committed to diversity, equity and inclusion (DEI)—it's not just the mission of WIE! We reflect this in our recently updated mission that further distills the goals and focus of the group. "The IEEE PELS WIE committee plays a vital role in fostering an environment of diversity and inclusion within PELS by hosting events and initiatives that support this commitment. It focuses on the development of events that support and welcome the entire community to be a part of the conversation" [1]. Today, PELS WIE is led by a steering committee whose members span countries and career fields that

spreads across all stages of academia and industry. Even if you don't identify yourself, events and resources will continue to be available to you and we encourage all PELS members to understand how they can become involved and leverage WIE resources.

Recently, the steering committee welcomed new members who are based in China, India, and Sri Lanka. The diversity of members and contributors helps us achieve a broader perspective on engagement and challenges facing members across the world, and as we continue to grow and serve the global community, voices from all IEEE Regions, including Region 10, will be of continued importance. The steering committee members and volunteers are engaged in doing everything from data analysis, writing articles, and volunteering at events. Since we're always, looking for new energy and excitement on the steering committee, the team will continue to grow into a more structured group to better serve PELS—check the end of the article for contact information and ways to get involved, or learn more about how you can help from wherever you are.

Recently, PELS WIE President Lauren Kegley reported on three pillars that flow directly from the PELS WIE mission statement [1]. These three key pillars lead us to report on three key areas of focus for the next few years:

1) **Advocacy for Equitable Elevation and Recognition: Data-Driven Approach to Improving Diversity**—The WIE team has made great strides in improving reporting on diversity within IEEE, starting with the PELS WIE

society, in order to quantify progress and gaps [2]. For us, diversity includes not just gender diversity, but also region, affiliations, race, ethnicity, and cultural identity, among others. The percentage of Women in PELS has more than tripled over the past decade [2] and IEEE PELS has set a goal to continually push this metric forward [3]. With a meaningful framework for tracking diversity metrics established with ways to shine a light on both areas with strong performance as well as areas for improvement, future work includes establishing metrics for IEEE diversity in the Fellows elevation process, and increasing members' access to peers and mentors for the goal of achieving elevation. If these topics interest you, please reach out to PELS@ieee.org.

2) **Education Events Targeted at Broad Demographics, Celebrating Diverse Voices: Professional Development**—While the pandemic created disruptions in our normal programming, these challenges also invited new opportunities. While travel was paused, we explored creative improvements to our virtual events that went beyond the webinar, making them even more interactive and exploring different mediums. For example, our "Mentors + Advocates" event included small group breakout sessions for improved networking and brainstorming about how you can nurture your relationships and find your next big supporter. Our "Power at the Table" series is designed to celebrate the stories

and voices of people changing the face of technology and also, provide career growth advice from leaders of diverse professions to engineering professionals in an accessible, fireside chat format. Our most recent event, a Fireside Chat with Electric C-Op CEO Curtis Wynn, is now available as a podcast. If you are unable to join an in-person event like the annual WIE event at the IEEE Applied Power Electronics Conference and Exposition (APEC), then you can join an online event or review previous events' materials and resources online. One ongoing popular topic is how to find mentors, advocates, and sponsors. Don't know what the difference is between all those roles? Check out the resources on the PELS WIE Events page [4] and push your career forward.

3) **Creating Networking Opportunities to Empower Diverse Voices & Authentic Expression of All Members: Conference and Outreach Events**—The PELS WIE group looks to share knowledge and collaborate beyond PELS WIE. In 2021, several PELS WIE steering committee members attended the WIE International Leadership Conference (ILC) interfacing with the broader IEEE WIE community, and also learning from women leaders from across industry holding leadership positions, including Stacey Abrams (US political activist), Sandra Rivera (Executive Vice President at Intel), and Susan Armstrong (Senior Vice President at Qualcomm). Connecting across the world is more vital than ever, and steering committee member Indhumathi Gunasekaran was able to network and learn from both leadership and technical

tracks, while also taking that experience to new forums by presenting on diversity and inclusion in India, as part of the IEEE PELS WIE event on International Diversity: “it was an excellent feeling to share my perspectives about how culture impacts diversity and inclusion” [5]. Another avenue for outreach in which IEEE PELS WIE is investing is

developing a resource for identification of diverse technical speakers in the power electronics field. In addition to building this database, the WIE steering committee can support local PELS chapters or other IEEE organizations to create a more diverse technical lecture series or to understand best-practices on how to develop inclusive events. If you are

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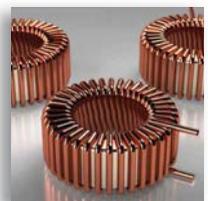
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interested in supporting this effort, please reach out to the IEEE PELS WIE committee at PELSWIE@ieee.org.

If you've been thinking about learning more or getting involved, there's no time like the present. A great place to start is the annual WIE breakfast at APEC, this year co-hosted with Young Professionals (YP) and Power Sources Manufacturers Association (PSMA). Held on March 22 at the conference, learn all the ways you can engage with PELS and PSMA, network with volunteers and officers, and uncover all the exciting opportunities behind these acronyms. More information on the events covered in this article, as well as information about future happenings, can be found at the PELS WIE page (<https://www.ieee-pels.org/wie>), or check out the *IEEE Power Electronics Magazine* website under "Society News" for a quick link. If you are interested in getting involved in WIE or DEI events, e-mail PELSWIE@ieee.org.

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Kristen Parrish (kristen@ieee.org) (Senior Member, IEEE) received the bachelor's degree from the Rose-Hulman Institute of Technology, Terre Haute, IN, USA, and the master's and Ph.D. degrees from The University of Texas at Austin, TX, USA, before embarking on a career spanning multiple fields, ultimately working in power electronics at both Texas Instruments, Dallas, TX, USA and Wolfspeed, Durham, NC, USA. Her work experience includes Research and Development Engineer, a Systems Engineer, and most recently as an Applications Engineer with projects in packaging, magnetics, and silicon carbide.

During her career, she has been involved with IEEE at the local section level, serving as the Eastern North Carolina Vice-Chair, the Women in Engineering (WIE) Chair, and the Webmaster, and also at the society level on the PELS WIE Steering Committee. She became a Senior Member of IEEE in 2020. She has also created a mentoring program that connected mentors and YP mentees in IEEE Region 3 during the early days of the COVID-19 pandemic, which was nominated for the MGA Young Professionals Achievement Award. She is passionate about mentoring and career development of women in engineering.

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Monolithic Bidirectional WBG Switches Rekindle Power Electronics Technology

There are numerous mass volume power applications where it is necessary to control the flow of bidirectional power, including electric vehicles (vehicle to grid, vehicle to home, and vehicle to vehicle), distributed and grid-tie power systems using regenerated energy and/or energy storage components, and solid-state circuit breaker protection. Silicon carbide (SiC) and gallium nitride (GaN) based bidirectional power switches can enable these applications with their compelling advantages of high efficiency, high blocking voltage capability, and low system weight and volume. In particular, monolithic switches that allow for bidirectional symmetric conduction and voltage blocking with a chip area close to that of a similarly rated unidirectional switch are ideally suited to fuel a revolution in power electronics technology.

Today, monolithic bidirectional (MBD) power semiconductor switches are not commercially available. Instead, back-to-back connection schemes of unidirectional power MOSFETs or IGBTs are typically used, resulting in a

4X penalty in chip area and high cost. However, various types of SiC and GaN bidirectional concepts are being investigated including bonded-wafer bidirectional IGBTs, monolithic dual-gate bidirectional GaN switches, and MBD back-to-back connected SiC MOSFETs and JFETs.

GaN power devices are commercially available from multiple vendors in the high volume ~650 V range. They are of lateral configuration and the gate-to-drain spacing determines blocking voltage capability. A high mobility lateral 2-D electron gas conducts current, and the lack of a body diode facilitates symmetric bidirectional current flow. GaN power devices are typically designed with a large

gate-to-drain spacing to withstand high voltage, and a smaller gate-to-source separation to accommodate the lower V_{GS} and save space on the wafer. This asymmetry only allows for unidirectional high voltage blocking. To enable symmetric bidirectional voltage blocking, equidistant source-gate and drain-gate spacings are required, which nearly doubles the size of the device. A more elegant MBD voltage blocking solution is the dual-gate structure of Figure 1 [1]. Sharing a common drain region reduces device cell pitch (lateral extent) and R_{on} , and only increases device area by about 1.2X compared to similarly rated commercial GaN unidirectional voltage blocking devices.

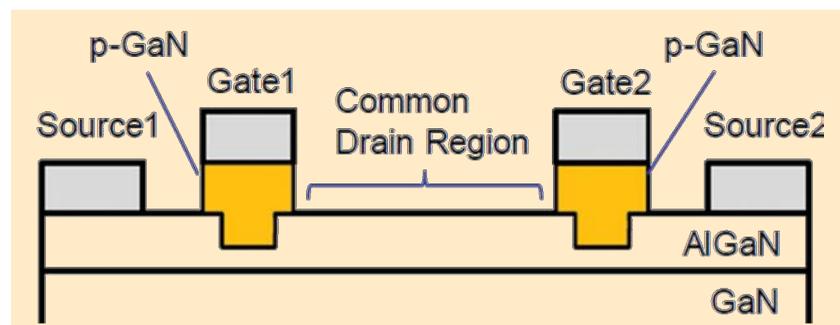


FIG 1 Monolithic bidirectional GaN switch with dual-gate structure. Sharing a common drain region reduces device cell pitch (lateral extent) and R_{on} .



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Recently, Panasonic demonstrated a prototype 1.1 kV, 100 A MBD GaN switch with dual-gate structure and R_{on} of 22 m Ω [2]. Infineon Technologies also demonstrated a similar monolithic dual-gate bidirectional GaN switch as part of their PowerAmerica project. Both Panasonic and Infineon have strong IP portfolios in this technology. Much like commercial lateral power GaN devices, their dual-gate bidirectional counterpart is fully silicon (Si) CMOS compatible and can be fabricated in volume fabs using mature node technology. This leverages existing Si economies of scale to reduce manufacturing cost.

Extending power device operation beyond 900 V might be impractical for GaN lateral devices as it necessitates larger lateral gate-to-drain separation, which reduces the total number of devices per wafer. It also requires growth of thick buffer layers, which can compromise thermal conductivity. Thus, for devices rated above 900 V, the vertical configuration is preferable as it optimizes space on the wafer. In vertical devices, blocking voltage is tailored by adjusting the doping and thickness of the vertical drift layer while the lateral device extent on the wafer remains approximately same (a small increase in device area with higher voltage rating is necessitated by the larger lateral extent of the edge termination). SiC power devices are vertical and the efficient choice for +900 V applications. They are commercially available to 3.3 kV from multiple vendors, with 6.5 and 10 kV MOSFETs having been demonstrated and inserted in engineering systems. Furthermore, SiC also competes effectively with GaN and Si IGBTs in the lucrative ~600 V EV and power supply applications space.

SiC MOSFETs and JFETs are capable of bidirectional symmetric current flow under appropriate biasing conditions. However, they only block voltage in the forward direction due to the gate and edge termination structures that are difficult to fabricate at both the device “bottom” and “top” to form a MBD switch with a single shared drift layer. In practice, bidirectional symmetric current-flow and voltage blocking have been demonstrated by connecting two SiC MOSFETs (or JFETs) in the anti-series (back-to-back) configuration schematically depicted in Figure 2. (See article in this issue “*The BiDFET Device and its Impact on Power Converters*” by B. Jayant Baliga, Douglas Hopkins, Subhashish Bhattacharya, Aditi Agarwal, Tzu-Hsuan Cheng, Ramandeep Narwal, Ajit Kanale, Suyash Shah, and Kijeong Han, *IEEE Power Electronics Magazine*, March 2023, p. 20)



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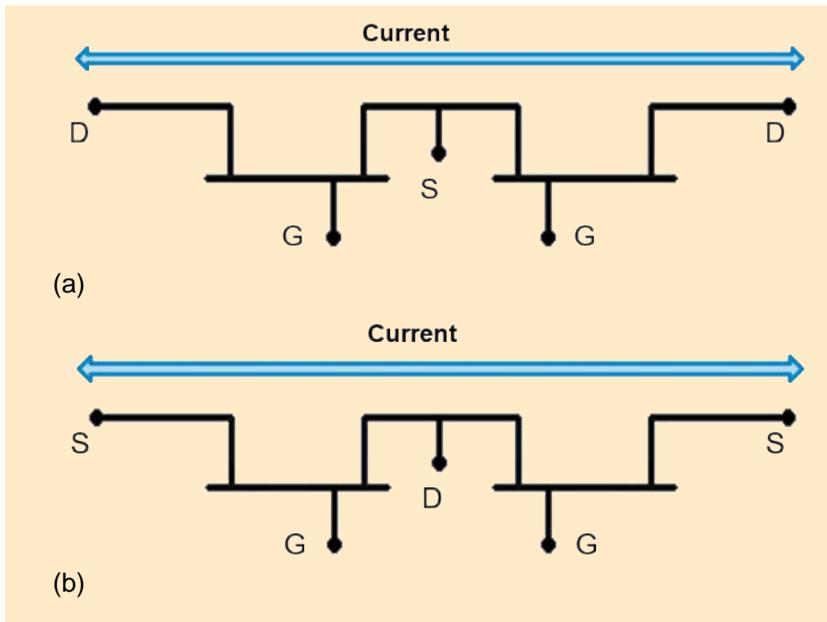


FIG 2 Back-to-back connected (a) common-source and (b) common-drain device configurations for symmetric bidirectional conduction and voltage blocking.

The common-source configuration of Figure 2(a) allows control of the bidirectional switch using a single synchronous drive signal to bias both gates [3]. Utilizing anti-series connected SiC JFETs, a bidirectional solid-state circuit breaker (BD-SSCB) with a single bipolar current actuated gate driver was demonstrated [4]. In no-fault circuit operation, current flows with all the JFET p-n junctions turned OFF. In a fault event, the reverse conducting JFET's gate-drain diode turns ON generating bipolar current that passes through the gate driver. The bipolar gate current was sensed in the driver to turn off the BD-SSCB. Despite being coupled with transient voltage suppression components to mitigate the

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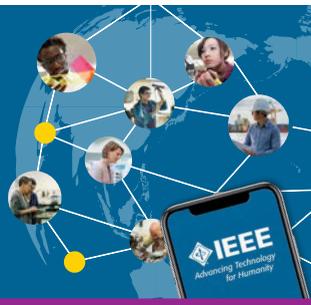
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fast SiC dV/dt , the BD-SSCB actuated three orders of magnitude faster than conventional mechanical circuit breakers and can provide dramatic improvements in reliability and operating life, resulting in superior system protection and reduced system maintenance and repair. The common drain bidirectional switch configuration of Figure 2(b) has recently been fabricated and tested in circuits [5]. The anti-series device configurations of Figure 2 can be monolithically integrated in a single chip on the wafer simplifying packaging and reducing parasitic inductances. SiC MBD fabrication utilizes the same processes of standard SiC switches, thereby exploiting that platform's volumes, yields, and performance metrics. Compared to similarly rated conventional unidirectional vertical MOS-FETs/JFETs, the bidirectional "two anti-series connected devices" configuration doubles total resistance. This is in contrast to the lateral GaN dual-gate bidirectional solution, where the common shared drift layer minimizes resistance. Indeed, for the "two anti-series connected devices" bidirectional SiC switch to equal the resistance of a single unidirectional device, the chip area must increase by 4X.

MBD switches provide opportunities for dramatically improving key performance metrics of dc-ac and ac-ac power converters, including their power density, efficiency, EMI suppression, and eventually cost. Three types of three-phase ac-ac converter topologies that are advantageously realized (high efficiency, high power density, and low circuit complexity) with MBD switches are indirect matrix converters, direct matrix converters, and current-source converters. While the compelling advantages of matrix converters for direct ac-ac power conversion have long been recognized, the unavailability of MBD switches has prevented matrix converters using the baseline 3×3 matrix of ac switches from achieving wide commercial success. Another opportunity for MBD switches is their application in a T-Type switching cell topology that provides the basis for designing high-performance SiC/GaN-based multi-level voltage-source inverters that can achieve appealingly high power density and efficiency. MBD switches also enable current-source-inverter based integrated motor drives, which combine motors and drives into the same housing, allowing for major improvements including higher power density and efficiency,

lower EMI, higher temperature operation, and enhanced fault protection in permanent magnet machine drives. (See article in this issue “*Monolithic Bidirectional Power Transistors: Opening New Horizons in Power Electronics*” by Jonas Huber and Johann W. Kolar, *IEEE Power Electronics Magazine*, March 2023, p. 28)

As SiC and GaN devices approach mass commercialization propelled by insertion in electric vehicles and consumer electronics, respectively, fabrication of SiC and GaN MBD switches is becoming economically viable enabling their wide adoption in key volume applications.

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Patent Law: A 30,000-Foot Aerial View

One of the enumerated powers granted to Congress by the U.S. Constitution is “[t]o promote the progress of science and useful arts, by securing for limited times to authors and inventors the exclusive right to their respective writings and discoveries.” U.S. Constitution, Article I, Section 8, Clause 8. A more straightforward read of this clause is that Congress has the power to confer, for limited times, exclusive rights to inventors for their discoveries and authors for their writings. Accordingly, Congress enacts legislation governing patents for inventors and copyrights for authors—thus, patent law and copyright law. This column focuses on patent law, which is codified in Title 35 of the U.S. Code (“35 U.S.C.”).

An inventor may keep his or her invention secret and hope to benefit from it indefinitely. This is the rationale behind trade secret protection (e.g., Coca-Cola’s Coke formula or KFC’s original recipe). But this inventor has no right to exclude someone, who independently conceives of the same invention, from making, using, offering for sale, selling, or importing the invention. The inventor may obtain such exclusionary rights [35 U.S.C. § 271(a)] for a limited time if he or she files an application (35 U.S.C. § 111) for a patent at the United States

Patent and Trademark Office (USPTO)—the federal agency established by Congress to issue patents on behalf of the government—and the USPTO grants him or her the patent for his or her invention.

There are three types of patents: utility, design, and plant. Utility patents are what most people have in mind when talking about patents and are likely more relevant to engineers reading this column. Utility patents may be granted to “[w]hoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof” (35 U.S.C. § 101). Hardware-related inventions typically fall under machine or manufacture, and software-related inventions under process. For a utility patent, the exclusionary rights last for 20 years from the date of filing the application [35 U.S.C. § 154(a)(2)]. When the patent expires, the invention is deemed to be part of the public domain for anyone to use freely.

To be clear, a patent does *not* grant an inventor the right to use his or her own invention, but grants him or her the exclusionary rights, which he or she may decide to enforce or not. An inventor does not have to use his or her invention covered by his or her patent to exercise the exclusionary rights. On the other hand, an inventor may choose to use his or her invention without seeking a patent, but assumes the risk of infringing

someone else’s patent that covers the invention. It is important to note that, in the U.S., if two or more inventors independently conceive of the same invention at different points in time, the *first inventor to file* an application for the invention will obtain the rights if granted a patent, regardless of whether she was the first one to conceive of the invention. For this reason, it is important to not delay filing a patent application.

After an application for a patent has been filed at the USPTO, it undergoes examination by an official known as an examiner. The examiner determines whether the application meets all the pertinent provisions of the law and merits a patent being awarded (35 U.S.C. § 131). For example, under 35 U.S.C. § 112, the examiner checks if the application adequately describes and clearly claims the invention. Importantly, the examiner determines if the invention is *patent-eligible* under 35 U.S.C. § 101 and *patentable* under 35 U.S.C. §§ 102 (novel) and 103 (nonobvious). For the invention to be novel, it must not be identically disclosed or described in a prior patent, publication, or other material available to the public—altogether often referred to as “prior art.” To be nonobvious, the invention must not have been within the capabilities of a person having ordinary skill in the art pertaining to the invention before the filing date of the invention.

In the upcoming column, I will go over what is known as patent prosecution—the process through which an inventor, or more commonly a patent professional (patent agent or attorney) representing the inventor, drafts and files an application and then negotiates with the USPTO/examiner in pursuit of a patent. In later columns, I will unpack several of the provisions of the law that I introduced above.

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Blockchain and Bitcoin: What It Means for Power Electronics

A perpetually hot topic in the news these days seems to be cryptocurrencies, and more broadly, blockchain technologies. After following some of the ups and downs from the past few months (and years), I wanted to take a look at where the technology has been and where it's headed—and how it will impact the power electronics industry. I'm not going to get too far into the details on how blockchain works here—for a deep dive into the technology, check out the November/December 2022 issue of IEEE Potentials: Blockchain Technology; Societal Impacts, Education and Research.

Blockchain technology was first proposed in 1982, as a method for cryptographers to implement tamper-proof document timestamping— independent trusted verification. It took over 25 years to apply this method to currency (kicking things off with the cryptocurrency Bitcoin), leveraging a decentralized method to record transaction logs on a “distributed ledger” for a virtual currency. Proponents point to this technology as an enabler of decentralized currencies that are not controlled by a centralized organization, such as a government. Of course, there are plenty of other cryptocurrencies floating around, from the meme-inspired Dogecoin which was at one time accepted by Tesla as legal

tender, to the now all-but-defunct FTX Token (FTT). These cryptocurrencies differentiate themselves slightly but since Bitcoin was the first, let's dive into the details about how Bitcoin transactions are powered—and why it's a big deal.

From a cryptography basics point of view, Bitcoin transactions and ‘mining’ (discovering of new blockchains that can be traded as Bitcoin) rely on a distributed network running checks on complex algorithms spread across a network. Back in 2009 at the beginning of Bitcoin, these calculations could be performed by individual users with home PCs, with some sources citing hundreds of bitcoins able to be mined every week on a single CPU. During this time, calculating a ‘winning’ block combination would yield

50 Bitcoins, a number that halves roughly every four years (it is currently 6.25 Bitcoins). In order to discover, or transact (buy/sell) Bitcoin currency, heavy computations must be performed that yield a fee to the ‘miner.’ There are 21 million Bitcoins available in total, as the original proposal had this cap feature in order to fix the supply, as a barrier against inflation. After more than a decade's worth of mining, there are just under 20 million Bitcoins in circulation—and the remaining lot is much harder (computationally expensive) to find. Figure 1 shows a brief overview of where we are now, compared to the beginning. As computing power has increased, and ASIC technology has matured down to now 7 nm CMOS process technology, energy efficiency has also increased.

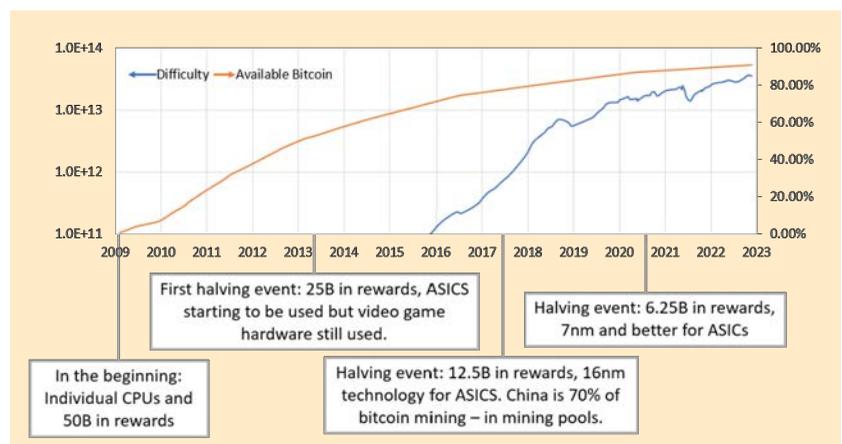


FIG 1 Difficulty and available Bitcoin over time. As more and more Bitcoin are found, the remaining sequences are increasingly difficult to achieve, with difficulty increasing by an order of magnitude every few years. Sources: CoinDesk.com, bitcoin.com.

Today, estimates show that one Bitcoin transaction takes nearly 1.5 MWh to complete (digiconomist). Embedded in this metric is the number of calculations required to complete a transaction, as well as hardware characteristics of the ASIC processor and power supply. Newer cryptocurrencies such as Ethereum and Solana are geared toward lower power consumption. While this 1.5 MWh figure may sound like a lot, depending on energy pricing at the moment, this can cost somewhere between \$20–\$100 USD, and Bitcoin price peaked last fall at around \$64,000 USD (at the time of this writing, the price is closer to 1/3 of that). Even if a transaction does not result in a new block or Bitcoin, miners are compensated with fees that can still outsize energy costs and motivate participation. Until the price of Bitcoin drops significantly, existing mining pools with no startup costs will still be able to find profits given

current typical energy rates. This power per transaction figure is not exactly the tidy number I was looking for to understand the tradeoffs for power hardware engineers given—these motivations are calculated from a complicated equation based on daily fluctuations in Bitcoin price and energy supply price, fighting against the increasing difficulty of mining new coins, offset by the continuing progress in hardware technology.

Zooming in on the hardware piece, let's take a look at the evolution of the supply chain in addressing Blockchain and cryptocurrency applications. Shortages of everything from power supplies to GPUs have come and gone as demand for these items for mining rigs have gone up and down with Bitcoin price. During this time, ASIC manufacturers are designing dedicated mining rigs, and the technology has gone from 130 to 7 nm, improving processing times, along with changing voltage rails and

dc-dc conversion). The volatility of Bitcoin, which tends to motivate day by day mining activities, has led to concerns about electronic waste, with some estimates suggesting hardware is upgraded every 1.5 years—compared to every 3–5 years for datacenter hardware, for example.

On the power supply side, besides the obvious push for efficiency, reliability, and the ability to handle high power draw is mission critical for miners and mining pools. While there hasn't been as clear a push for cryptocurrency mining specific designs, compared to ASICS, there are a few semiconductor reference designs from Texas Instruments, and Transphorm has publicized its 650 V GaN FETs in a 3.6 kW power supply geared toward crypto mining.

On the energy source side, discussions of how these mining activities are being powered are another hot topic. Mining pools have sprung up across the world around sources of

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renewable (and inexpensive) energy. At one point, city governments in Sichuan, China, were encouraging crypto miners to set up camp locally in order to use extra hydroelectric power generated by dams during the rainy season. However, in 2021, the People's Republic of China (PRC) government completely banned all cryptocurrency transactions, resulting in sell-offs of some of the smaller

hydroelectric plants that had been bought by mining pools. Big hotspots for mining today are countries such as Canada and Iceland, with the USA claiming the biggest share of Bitcoin mining activity (Kazakhstan and Russia are second and third).

Bitcoin advocates will point out that the often-cited power-per-transaction number can be misleading without context, and that existing

financial systems based on physical currencies, as most world governments currently operate, also use significant amounts of power. And while the shift and strategic use of renewables can offset carbon footprint, there is opportunity cost of not using these resources towards power generation for cities, for example. As regulations increase and standardization matures, it may become more easy to quantifiably compare cryptocurrency technologies, especially from a power and energy point of view.

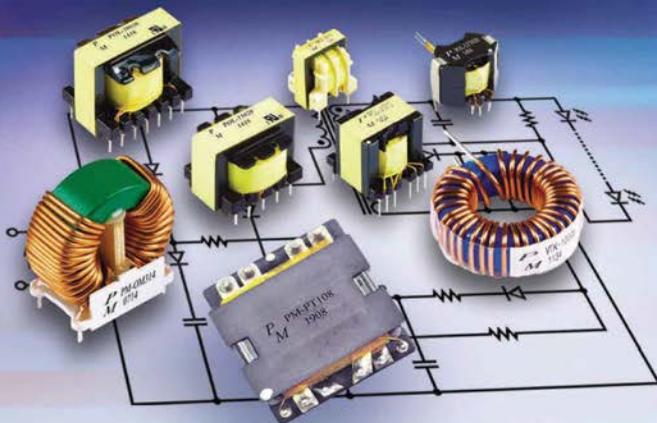
At least in the near future, I don't expect cryptocurrency and blockchain technologies to disappear from the news. But, it remains to be seen how regulation and standardization will shape up to get us better understanding of the power and energy implications of this technology. As the technology develops, I'm interested to see how it will be applied to other fields such as our own. History has shown that some of the most impactful innovations happen when two seemingly disparate technologies join together to make something radically new. Since it took 25 years to go from the original blockchain idea to the application that everyone can't stop talking about, I'm curious to see where we'll go next.

About the Author

Kristen Parrish (kristen@ieee.org) has worked in the field of power electronics for six years, with a career spanning RF, mmWave, photonics, and packaging. Drop her a line and let her know what you are interested in seeing from the column, or if you have any industry news to share—you can reach her at kristen@ieee.org, or visit her website at kristenparrish.com.



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by Haifah Sambo, Anshuman Sharma,
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Explore the IEEE PELS Students and Young Professionals Committee and Get Involved

Over the last years, the number of student and young professional members in IEEE PELS has increased. Students and young professionals now represent over 20% of the membership body and make significant contributions to the dynamism of IEEE PELS. Via the IEEE PELS Students and Young Professionals (S&YP) committee, a subgroup within the PELS membership committee, students and recent graduates in IEEE PELS host a variety of events at IEEE conferences and create activities to engage PELS members while enabling unique networking and mentorship opportunities. With volunteers all across the globe (Algeria, Brazil, Canada, Germany, India, Portugal, Spain, Sri Lanka, and the United States), the S&YP committee also establishes a global and inclusive community for engineers, researchers, academics and students in the area of power electronics. Through its endeavors, the S&YP committee aims to support the professional development of students and recent graduates, further the mission of IEEE PELS and increase the

diversity of its membership and volunteering bodies.

The Student Activities Committee (SAC) is a sub-unit of the IEEE PELS S&YP committee and was founded in February 2019. The committee engages in active discussions to propose and implement relevant solutions to address the issues faced by PELS students and Student Branch Chapters (SBCs). Additionally, the committee initiates specific programming focused on student members with the SAC's mission being to deliver quality student membership experience to the PELS students across the world and provide diverse opportunities to the IEEE PELS student members to collaborate and contribute back to the society.

Events and IEEE Conferences

The S&YP committee regularly hosts receptions at leading international power electronics conferences. The IEEE Energy Conversion Congress and Exposition (ECCE North America), the International Power Electronics Conference (IPEC ECCE Asia), the European Conference on Power Electronics and Applications (EPE ECCE Europe), the IEEE Transportation

Electrification Conference and Exposition (ITEC), and the IEEE Applied Power Electronics Conference and Exposition (APEC) were all previous venues of PELS Young Professionals receptions.

Outreach and collaboration being key values of IEEE PELS and its S&YP committee, many events are hosted in partnership with other organizations (Figure 1). At ITEC 2022 held in Anaheim, CA, USA, the S&YP committee collaborated with the IEEE Industry Application Society (IAS) to organize a networking reception. With over a hundred attendees, the networking reception gathered students and young professionals from academic, industry and research entities over valuable exchanges, great food and memorable southern Californian weather. At APEC 2022 held in Houston (TX), USA, the S&YP committee collaborated with IEEE PELS Women in Engineering (WIE) and the Power Sources Manufacturers Association (PSMA) to organize a breakfast discussion titled "How to become involved with IEEE PELS and PSMA too." A similar breakfast discussion was also hosted at ECCE 2022 in Detroit (MI), USA.



FIG 1 PELS Young Professionals reception during the 24th edition of EPE ECCE Europe (EPE'22 ECCE Europe) held at the beautiful Welfenschloss at Leibniz University Hannover. Source: Nazariy Kryvosheyev.

In the future, the S&YP committee intends to continue hosting receptions at IEEE conferences and collaborating with other organizations to enable students and young professionals to network with members of various IEEE PELS subgroups. S&YP receptions will be renewed this year at the upcoming APEC 2023, ECCE North America 2023, IPEC ECCE Asia, and ITEC 2023 conferences. Furthermore, the IEEE PELS Shanghai Chapter is organizing the second PELS Students and Young Professionals Symposium (SYPS 2023) with the full support of the PELS Membership

Committee—China and the IEEE PELS S&YP committee. This event will be centered around the publications, presentations, and demonstrations of IEEE PELS students and young professionals.

Engagement Activities

In addition to connecting IEEE PELS members with one another through networking and receptions, the S&YP committee encourages PELS members to participate in convivial and community-oriented activities. Trivia quizzes and raffles are often conducted during celebratory events and conference receptions as

well as on IEEE PELS social media platforms. On IEEE PELS's 35th birthday in June 2022, the S&YP committee organized an anniversary logo redesign contest. Many submissions were entered and the two top winning propositions were publicly acknowledged and recompensed with cash prizes. The annual PELS Day photo contest, hosted for the past three years, has become an S&YP committee tradition. Every year, various IEEE PELS student chapters use their creativity to submit the most impressive photograph of their members showcasing the colors and symbols of IEEE PELS. Every year, the PELS Day photo contest unifies students within their chapters to celebrate IEEE PELS locally (Figure 2).

The success of these engagement activities in 2022 has inspired the S&YP committee members to increase such events in the future. In addition to the traditional PELS Day photo contest, the S&YP committee aims to establish conference photo contests with APEC 2023 being the first venue for this new competition.

Conclusion

The events and activities organized by the S&YP committee are intended to further its ultimate goal “helping students and recent graduates transition to young professionals within the larger framework of the IEEE community, specifically the PELS community.” Networking and community building being necessary tools for career and professional development, the S&YP committee is dedicated to creating opportunities for students and young

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FIG 2 A photograph submitted by the PELS SBC at NSSCE, India, for the 2022 PELS Day photo contest.

professionals to meet, connect, and exchange with each other and other PELS members.

The S&YP committee is also dedicated to diversifying its membership and volunteering bodies, as well as creating inclusive spaces. IEEE PELS social media platforms are heavily leveraged in the promotion of events and activities to ensure members from all across the globe are taking advantage of the opportunities offered by the organization. Special attention is also given to recruiting volunteers of diverse identities and backgrounds in the hopes that all students and young professionals in IEEE PELS can feel represented in the S&YP committee.

The S&YP committee is always seeking motivated volunteers. If interested in volunteering, please contact the S&YP committee chair, Nayara Brandão de Freitas, at nayara@ieee.org.

To stay updated with IEEE PELS and its S&YP committee, follow us on Twitter (@ieeepels),

Instagram (@ieeepels), and LinkedIn (IEEE Power Electronics Society).

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IEEE PELS China Membership WIE Subcommittee Co-Sponsors WIP Forum

On 10 December 2022, the Women in Engineering (WIE) Subcommittee of the IEEE Power Electronics Society (PELS) China Membership Committee co-sponsored the Women in Power (WIP) forum at the 4th International Conference on Smart Power & Internet Energy Systems (SPIES2022). The forum had the theme “Facing the Challenges of Modern Power Systems-Inspiring

More Female Engineers” and was held online.

To begin the event, Dr. Ruomei Li (former chair of IEEE Power and Energy Society (PES) and WIP), Prof. Hua Geng (general chair of SPIES2022), and Prof. Zhaohong Bie (chair of IEEE PES China Chapter) delivered an opening speech. There were multiple sessions made up of keynote speeches, panel discussions, and presentations of awards. During the last two sessions, six experts from both academia and industry shared cutting-edge research work

around the challenges of modern power systems and their experience on the dilemmas and opportunities encountered by female scientists.

At the last session, two rewards were presented by Prof. Bie. The first award was the Excellent Women Award and was given to Dr. Li to thank her for her long-term encouragement, support, and love for female engineers. The second award was the Excellent Paper Award of the WIP Forum and was given to three female researchers for their outstanding papers published at the conference.

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Date of publication: 3 March 2023

by Yinka Leo Ogundiran

IEEE PELS/IAS Sheffield SBC Hosts Special IEEE Day Guest Lecture

On 24 October 2022, the IEEE Power Electronics Society (PELS)/Industry

Applications Society (IAS) Sheffield Student Branch Chapter (SBC) and the Electric Machines and Drives (EMD) Research Group hosted a guest lecture titled “Automotive Servo Drives” by Dr. David Moule

(ZF Group, Germany) in honor of IEEE Day.

Prof. Z. Q. Zhu (Head of EMD Research Group) began the event with some brief remarks and then introduced Dr. Moule to the

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audience. During his presentation, Dr. Moule discussed the technical challenges associated with the design of automotive servo drives for the increasingly unfolding trend of autonomous electric vehicles (EVs), which are interconnected (Figure 1). He explained how optimization and better space utilization could be facilitated by making EVs to be autonomous and described the innovative techniques that could minimize clogging torques and ripple in electrical machine design, which could make them more suitable for adjustable speed drives in the future.

The presentation was followed by a question-and-answer session.



FIG 1 Dr. Moule giving his presentation.

The IEEE PELS/IAS Sheffield SBC and the EMD Research Group would like to thank Prof. Zhu for

coming as a guest lecturer and giving an informative and insightful presentation.

by Vladimir Katic

IEEE IAS/IES/PELS Serbia Joint Chapter Organizes Ph.D. Students Workshop

On 16 December 2022, the IEEE Industry Applications Society (IAS)/Industrial Electronics Society (IES)/Power Electronics Society (PELS) Serbia Joint Chapter organized and hosted the first Ph.D. students workshop with the topic “Research Trends in Power Engineering,

Power Electronics, and Applied Computing at the Faculty of Technical Sciences” and consisted of short presentations and extensive discussions. The goal was to bring doctoral students together and to show the latest directions for their research.

Six Ph.D. students presented their research trends and results: Milica Banović on “Diagnostics and Efficiency in Modern Energy

Conversion Applications,” Mladen Vučković on “The Possibility of Developing a Model of a PMSM Without Inductance Modeling but Using Flux Maps, i.e. Inverse Flux Maps,” Suleiman Milad on “The Possibilities of Wind Energy in Libya,” Radovan Turović on “Smart Preservation of the Power Quality in Distribution Networks,” Nebojša Horvat on “Blockchain Application in the Power Industry,” and Jovana

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FIG 1 Participants at the Ph.D. Students Workshop.

Jovanović on “Blockchain Visualization” (Figure 1).

Throughout the discussions, different views and new ideas emerged, allowing students to receive suggestions for improving their research and more efficient use of laboratory and computing facilities. The workshop also gathered students’ supervisors, advisors, and other researchers who shared their knowledge and experience with the students. The IEEE IAS/IES/PELS Serbia Joint Chapter is pleased with the success of the event and is looking forward to planning more in the future.

by Yingqi Liang

IEEE Joint IAS/PELS/PES SBC at NUS Organizes Two Programs

The IEEE Joint Industry Applications Society (IAS)/Power Electronics Society (PELS)/Power and Energy Society (PES) Student Branch Chapter (SBC) at the National University of Singapore (NUS) recently organized two guest lecturer programs.

For the first program, Prof. Subhashish Bhattacharya (North Carolina State University, Raleigh, NC, USA) gave a lecture on the topic “Solid State Transformer Journey – From Concept to Pilot Demonstration in a Decade, and Solid State DC Transformers for DC Grids” on 22 November 2022. The

presentation chronicled the Solid State Transformer journey from concept to pilot demonstration in a decade.

The second program took place on 25 November 2022. The lecture was

presented by Prof. Udaya K. Madawala (University of Auckland, New Zealand) on the topic “Advances in Wireless Power Transfer Technology” (Figure 1). Prof. Madawala highlighted the recent advances in



FIG 1 Prof. Madawala presenting his lecture on 25 November 2022.

wireless power transfer systems, new circuit and magnetic modeling techniques, and the concepts of an optimal control strategy.

Both events sparked discussions among the attendees, who appreciated the lectures. The SBC would like to thank both Prof. Bhattacharya

and Prof. Madawala for presenting lectures at NUS and is looking forward to organizing more events in the future.

by Drazen Dujic

IEEE PELS Swiss Chapter Workshop on Power Electronics in Robotics

The IEEE Power Electronics Society (PELS) Swiss Chapter organized a technical workshop in October 2022 that focused on the role and importance of power electronics in robotics. The event was held in Technopark, Zurich, Switzerland and was hosted and sponsored by PLEXIM.

During the event, several talks were given by various experts. The first industrial presentation was by Dr. Mario Maurerer and Dr. Gabriel Ortiz from ANYBOTICS and focused on a four-legged robot that could be used for industrial and hazardous inspection applications. For the second industrial presentation, Dr. Alexander Tschesno and Mr. Nikos Chrysogelos from FOTO-KITE shared their tethered drone that is used for situational awareness and is currently used by firefighters. Afterward, two talks were given by scientific researchers at the Ecole Polytechnique Federale de Lausanne in Switzerland. Dr. Alessandro Crespi presented the



FIG 1 Attendees at the workshop and some of the demonstrations.

evolution of the ENVIROBOT, which is a research platform bio-robot that has a swimming ability, allowing it to be used for water collection and analysis. Mr. Ali Reza Manzoori presented the research and development of the lower-limb exoskeletons in medical assistance, augmentation, and rehabilitation applications.

After the presentations, there was an engaging panel discussion with speakers along with practical demonstrations (Figure 1). Around 40 participants attended the event. The IEEE PELS Swiss Chapter would like to thank PLEXIM for sponsoring a successful event and is looking forward to organizing more such events in the future.

IEEE Joint IES/IAS/PELS German Chapter Organizes Student Summit

From 2 to 4 November 2022, the IEEE Joint Industrial Electronics Society (IES)/Industry Applications Society (IAS)/Power Electronics Society (PELS) German Chapter organized the Power Electronics Student Summit (PELSS), which was hosted by the Bonn-Rhein-Sieg University of Applied Sciences at the University of Kassel and Fraunhofer IEE. The conference is a specialist conference that enables undergraduate and graduate students to gain initial experience in preparing, publishing, and discussing their own research work in front of a specialist audience.

About 50 participants and 30 papers with presentations were a

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FIG 1 Attendees at PELSS.

part of the program (Figure 1). The papers that were presented will be published in IEEE Xplore. PELSS also had an industry exhibition, which included visits to the

Fraunhofer IEE Lab and the SMA Solar Technologies AG. The Chapter would like to thank its participants, supporters, and sponsors for a successful event.

by Ronald G. DeLuca

IEEE PELS Long Island Chapter Hosts Fourth Annual Power Electronics Symposium

On 3 November 2022, the IEEE Power Electronics Society (PELS) Long Island Chapter hosted its fourth annual Power Electronics Symposium (PES) at the Radisson Hotel in Hauppauge, New York, USA. The event hosted over 50 exhibitors who

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featured a range of power products and services.

For the keynote address, Dr. Fang Luo (Stony Brook University, USA) focused on the leading-edge research in power electronics at the university. The symposium also had eight presentations from industrywide companies featuring a host of power topics, including circuit design and analysis, circuit simulations, GaN high-electron mobility transistors, magnetic

design, power semiconductors, and SiC devices.

Over 450 power professionals from the Long Island and New York metropolitan area attended the event and were able to receive PDH and CEU credits for each presentation. The IEEE PELS Long Island Chapter is happy with the success of this event and looking forward to the next PES in 2023.



2023

13–14 February

College Station, TX, USA

IEEE Texas Power and Energy Conference (TPEC)

<http://tpec.engr.tamu.edu/>

19–21 February

Luxor, Egypt

IEEE Conference on Power Electronics and Renewable Energy (CPERE)

<https://www.ieee-cpere.org/>

2–3 March

Champaign, IL, USA

IEEE Power and Energy Conference at Illinois (PECI)

<https://www.peci.ece.illinois.edu/>

19–23 March

Orlando, FL, USA

IEEE Applied Power Electronics Conference and Exposition (APEC)

<http://www.apec-conf.org/>

29–31 March

Venice, Italy

IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)

<http://www.esars-itec.eu/>

19–21 April

Denver, CO, USA

IEEE Green Technologies Conference (GreenTech)

<https://ieeegreentech.org/>

27–28 April

Manhattan, KS, USA

IEEE Kansas Power and Energy Conference (KPEC)

<https://www.kpec-ksu.org/>

15–18 May

San Francisco, CA, USA

IEEE International Electric Machines & Drives Conference (IEMDC)

<https://www.iemdc.org/>

22–25 May

Jeju-do, South Korea

11th International Conference on Power Electronics and ECCE Asia (ICPE 2023–ECCE Asia)

<http://www.icpe-conf.org/>

28 May–1 June

Hong Kong

35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)

<https://ispsd2023.com/>

1–4 June

Wuhan, China

IEEE International Conference on Predictive Control of Electrical Drives and Power Electronics (PRECEDE)

<http://www.precede2023.com/>

4–8 June

San Diego, CA, USA

IEEE Wireless Power Technology Conference and Expo (WPTCE)

<https://ieee-wptce.org/>

9–12 June

Shanghai, China

IEEE 14th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)

<http://www.ieee-pedg2023.org/index.html>

21–23 June

Detroit, MI, USA

IEEE Transportation Electrification Conference & Expo (ITEC)

<https://itec-conf.com/>

25–28 June

Ann Arbor, MI, USA

IEEE 24th Workshop on Control and Modeling for Power Electronics (COMPEL)

<https://ieee-compel.org/>

18–19 July

Nottingham, United Kingdom

IEEE Workshop on Power Electronics for Aerospace Applications (PEASA)

2–4 August

Old Town Alexandria, VA, USA

IEEE Electric Ship Technologies Symposium (ESTS)

<https://ests.mit.edu/>

16–18 August

Seoul, South Korea

IEEE International Symposium on Sensorless Control for Electrical Drives (SLED)

28–31 August

Chania, Greece

IEEE 14th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED)

<https://www.ieee-sdemped.org/>

1–3 September

Izmir Cesme, Turkey

Joint International Aegean Conference on Electrical Machines and Power Electronics (ACEMP) & International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)

<http://acemp.metu.edu.tr/>

4–6 September

Mugla, Turkey

International Conference on Smart Energy Systems and Technologies (SEST)

<http://www.sest2023.org/>

24–26 September

Miami, FL, USA

IEEE Design Methodologies Conference (DMC)

<https://attend.ieee.org/dmc-2023/>

12–15 October

Radnor, PA, USA

IEEE Global Humanitarian Technology Conference (GHTC)

<https://ieeeghtc.org/>

29 October–2 November

Nashville, TN, USA

IEEE Energy Conversion Congress and Exposition (ECCE)

<https://www.ieee-ecce.org/2023/>

15–17 November

Auckland, New Zealand

IEEE Fifth International Conference on DC Microgrids (ICDCM)

26–29 November

Florianopolis, Brazil

IEEE 8th Southern Power Electronics Conference (SPEC)

4–6 December

Charlotte, NC, USA

IEEE 10th Workshop on Wide Bandgap Power Devices & Applications (WiPDA)

14–16 December

Guwahati, India

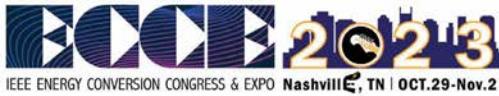
11th National Power Electronics Conference (NPEC)

2024

25–29 February

Long Beach, CA, USA

IEEE Applied Power Electronics Conference and Exposition (APEC)



ECCE 2023

Nashville, Tennessee
October 29 – November 2, 2023.

About The Conference

The five-day IEEE Energy Conversion Conference and Expo will be held at the Music City Center in Nashville, Tennessee | October 29 – November 2, 2023. ECCE is the pivotal international conference and exposition event on electrical and electromechanical energy conversion field.



Day Care On-site

ECCE 2023 is an experience for everyone, and that means parents too! If your child is still a bit too young to appreciate the complexity of High power/voltage power conversion (HVDC, FACTS and multi-terminal DC systems) we've got you covered!



Confirmed Keynote

Elif Balkas
Chief Technology Officer, Wolfspeed

As Chief Technology Officer, Elif focuses on pioneering breakthrough semiconductor technology for Wolfspeed's Power and RF commercial applications.



Student Activities

No matter if you are a graduate student or an undergraduate student ECCE 2023 offers a variety of opportunities for you including student attendance grants, project demonstrations, job fairs, and more! Launch your career to the next level at IEEE ECCE 2023, in Nashville Tennessee. For information about student deadlines and more, visit our website!



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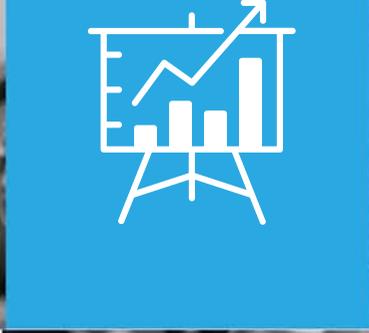
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ITEC
2023



2023 IEEE Transportation Electrification Conference & Expo



June 21- 23, 2023
Detroit, Michigan

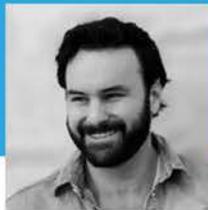
Keynote Speakers :

About ITEC

For more than 10 years, ITEC has served as IEEE's premier conference on transportation electrification, fostering connections between industry and academia. This year's conference will be held from June 21-23, 2023, at the newly renovated Huntington Place Convention Center.



Zafer Sahinoglu
General Manager at Mitsubishi
Electric Innovation Center



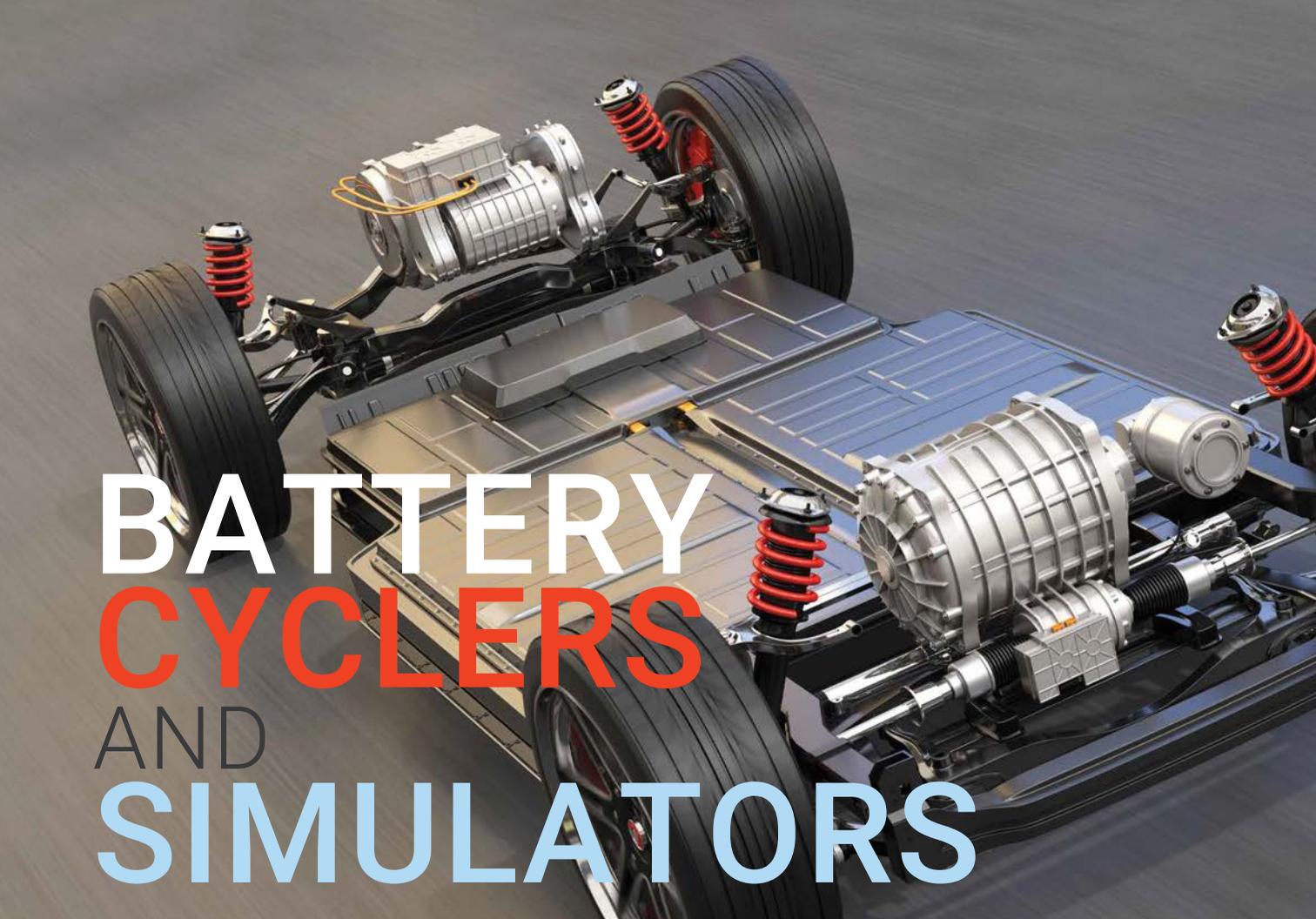
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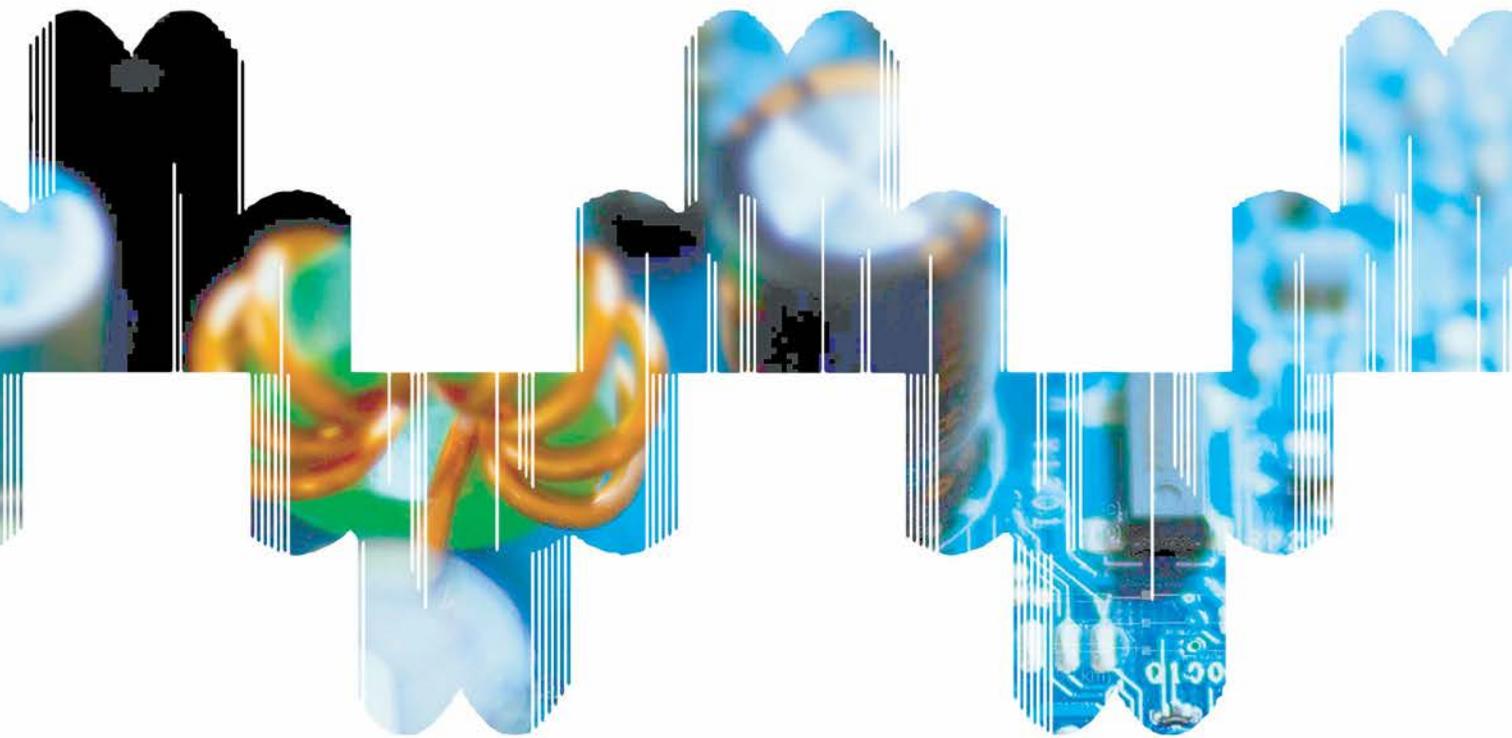


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