POWER ELECTRONICS NEWS

MAY 2023

Rethinking Power MOSFET Design for Greater Efficiency and Performance

Infineon

VIEWPOINT

Increasing the Pace of Our Search for Greater Efficiencies

With a focus on high-switching–frequency applications like telecom SMPS and solar energy systems, semiconductor technology holds immense potential for bringing significant improvements to various other application fields. In this issue, Infineon introduces its OptiMOS 6 device technology—a novel cell-design approach for higher power densities and cost-effectiveness. The advances in overall device performance led to the creation of a device structure to employ a 3D charge compensation in conjunction with a metal gate in a trench power MOSFET. As a result, this technology reduces on-resistance, dramatically lowers gate- and gate-drain charges and improves switching homogeneity across the device area. These achievements translate into a significant enhancement in system efficiency in various applications across different load conditions.

Today, silicon carbide is used in demanding semiconductor applications like trains, turbines, electric vehicles and smart grids. Because the market aims for power-device price parity with Si-based devices, SiC substrate producers are motivated to increase process efficiency and lower wafer-production costs. Additionally, SiC-based applications and all other types of semiconductors are in extremely high demand, necessitating innovation in the manufacturing process. In this issue, we analyze Pureon's semiconductor experience with its own polishing and surface laboratories. Ranbir Singh, executive vice president, and Siddarth Sundaresan, senior vice president of SiC technology and operations, both at Navitas Semiconductor, will analyze how all-SiC inverters will revolutionize electricity delivery, renewable-energy integration and energy storage.

In automotive and industrial applications, the need for high power has increased in modern electronics. Kilowatt-power output is a typical requirement for applications like motor drives, inverters or on-board chargers. This means the need to handle greater power is being transferred to the components, especially MOSFETs, due to existing space constraints in modules. An article in this issue analyzes LFPAK technology and how it addresses the challenging requirements coming from power electronics applications.

As the world shifts to increased renewable energy, a transformation is occurring in the storage and conversion of this energy for everyday household use. An article in this issue focuses on a presentation delivered by Jacob Mueller, a senior member of the technical staff with the energy storage technology and systems department at Sandia National Laboratories, on the key trends and challenges involved in this transformation, focusing on the role of power electronics and energy storage. Other topics analyzed in this issue are fusion energy, how GaN reliability is validated, SiC technology for electrification and a deep dive into STMicroelectronics' third-generation automotive-grade SiC MOSFETs. Moreover, contributing writer Katherine Bonamo analyzes semiconductor manufacturing from a sustainable point of view.

Yours Sincerely,
Maurizio Di Paolo Emilio
Editor-in-Chief, Power Electronics News

The AspenCore Guide to

Gallium Nitride

This 150+ page book on **Gallium Nitride (GaN)** power devices provides a comprehensive look at the technology, applications, market, and future of this emerging wide-bandgap material for power electronics.

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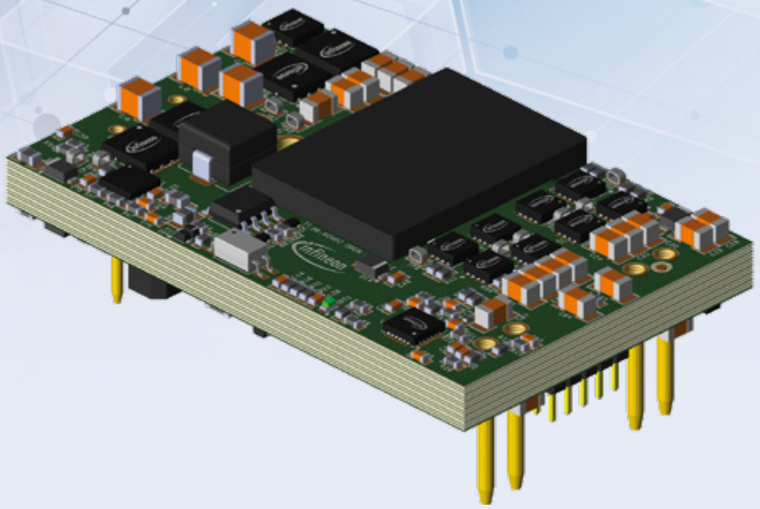

Accelerating the Drive for Higher Efficiencies Through Power MOSFET Technology Innovation

Introducing Infineon's latest OptiMOS™ 6 device technology—a novel cell-design approach for higher power densities and cost-effectiveness

*By **Ralf Siemieniec**, Senior Principal Engineer Power Device Development; **Simone Mazzer**, Senior Engineer Product Applications; **Cesar Braz**, Principal Engineer Product Definition; **Michael Hutzler**, Lead Principal Engineer Technology Development; **David Laforet**, Lead Principal Engineer Technology Development; **Ingmar Neumann**, Principal Engineer Technology Development; **Elias Pree**, Senior Staff Engineer Technology Development; and **Alessandro Ferrara**, Principal Engineer Product Concept, all at Infineon Technologies*

MOSFET technology has been widely recognized as an excellent option for switches in power management circuits since its inception. Commercially available since the late 1970s, vertical diffused MOSFET (VDMOS) structures were the first to fulfill the need for a power switch.[1] Due to its superior switching performance and high input impedance, the MOSFET quickly emerged as an attractive alternative to bipolar technologies. However, its application in the power electronics industry was limited by the high on-state resistance that restricted the current-handling capabilities of the VDMOS. In medium-voltage VDMOS, the intrinsic channel resistance and the JFET region—which restrict the channel current flow into the epitaxially-grown drift region—were the primary contributors to the total on-state resistance ($R_{DS(on)}$) between the drain and source (Figure 1a).

It took more than a decade of device design and process engineering progress to overcome this limitation, which finally led to the commercialization of the first trench-gate MOSFETs in the late 1980s. By moving the channel in the vertical direction, this device concept enabled a reduction in cell pitch without negatively affecting current spreading. The virtual elimination of the JFET region dramatically decreased the on-state resistance (Figure 1b). Nevertheless, the significant increase in cell density not only established the trench MOSFET as a competitive alternative to planar technology but also brought substantial drawbacks to light.

The gate-drain capacitance (related to trench-gate penetration in the epi drift region) and gate-source capacitance (overall capacitance between trench gate and body/source diffusion) increase linearly with the number of trenches, i.e., with the cell density. Together with a sublinear scaling in the on-resistance, this significantly impacts the technology figure of merit (FOM) $FOM_g = R_{DS(on)} \times Q_g$. Because the MOSFET is uniquely controlled through its gate terminal, the gate-driver circuitry has to provide the total gate charge (Q_g) required to turn on the transistor. In the case of high-switching–frequency applications, the lowest gate charge is desirable, as it proportionally reduces the driving losses. A part of the total gate charge is associated with the gate-to-drain charge (Q_{gd}), which governs the drain-voltage transient. A higher Q_{gd} impacts the transient speed, increases the switching losses and forces the use of longer deadtimes. It became evident that specific measures were needed to reduce the overall gate and gate-drain charge.

A new era started with the introduction of charge-compensated structures, exploiting the same principle as superjunction devices. Introducing devices that use an insulated deep field plate as an extension of the gate electrode enabled the lateral depletion of the drift region in the off state (Figure 1c).[2] The lateral depletion alters the electric field distribution throughout the structure, allowing the same voltage to be blocked within a shorter length. Because the electric field can now be supported by a thinner and more heavily doped drift region, a substantial reduction in the on-state resistance can be achieved. It is worth noticing that the field plate (as an extension of the gate electrode) leads to both a significant increase of the reverse-transfer capacitance C_{gd} (hence also Q_{gd} and Q_g) and a nonlinear dependence on the drain voltage.

In fact, the transfer capacitance drops abruptly as soon as the mesa region completely depletes. These disadvantages were soon overcome by using a field

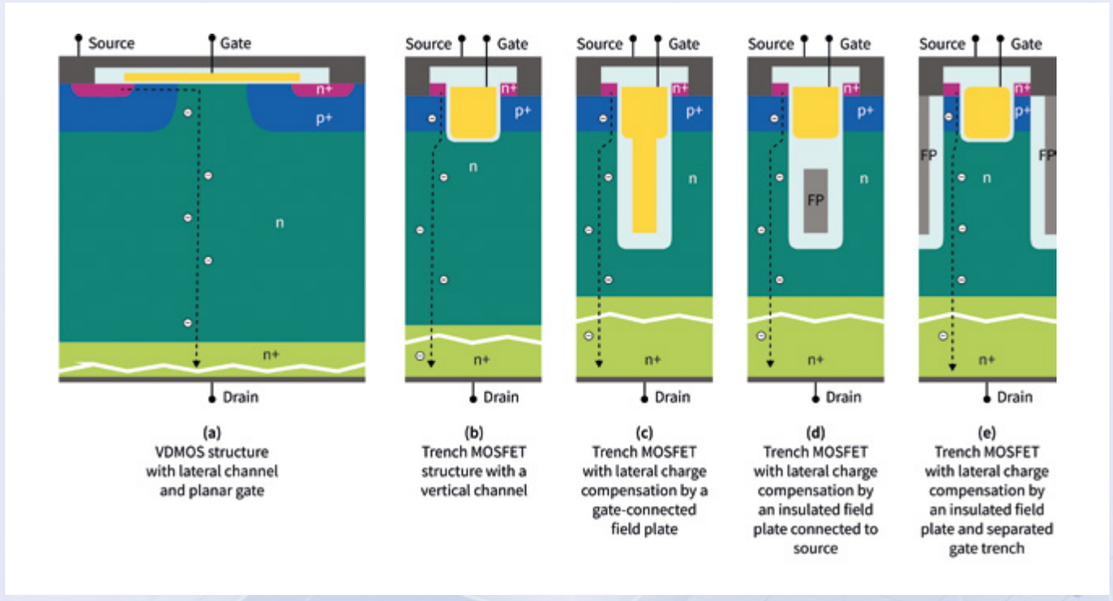

Figure 1: Exemplary device structures depicting the evolution of a power MOSFET

plate, which was isolated from the gate electrode and instead electrically connected to the source potential (Figure 1d). While the charge compensation principle operates as before, the buried field plate does not introduce any additional contributions to the gate-drain capacitance. Instead, the field plate shields the gate electrode from the drain potential, which reduces the gate-drain capacitance C_{gd} and related charges. These devices, at the time of their introduction to the market, showed best-in-class performance with low gate charge and gate-drain charge characteristics, high switching speeds and good avalanche ruggedness.[3]

INFINEON'S INNOVATIVE APPROACH TO RAISING POWER MOSFET DESIGN TO THE NEXT LEVEL

To reach the next level in power MOSFET evolution, new MOSFET devices are required to provide improvements across all FOMs. This is needed to enable high-frequency switched-mode power supply (SMPS) operation, whereby losses are associated with charges (switching) and on-state resistance (conduction). To meet these more demanding requirements, a novel cell-design approach has been developed and implemented, which explores for the first time a true 3D charge compensation.

First, a direct connection of the field-plate electrodes to the top-side source metal is required, as illustrated in Figure 1e. Second, the device layout must move away from the common stripe layout to a grid-like layout structure, as depicted in Figure 2. This increases the silicon area for current conduction compared with a structure with stripes, allowing a further reduction of the overall on-resistance in the new ***OptiMOS™ 6 low- and medium-voltage power MOSFETs***. In order to also further reduce the $FOM_g = R_{DS(on)} \times Q_g$ and $FOM_{gd} = R_{DS(on)} \times Q_{gd}$ values, the gate trench underwent a complete redesign to minimize its lateral extension. However, the substantially smaller dimensions of the gate impose a new challenge, as the use of polysilicon as gate material would result in unacceptably large internal gate resistances. The introduction of gate fingers usually solves this issue, but these reduce the active area available for current conduction.

Instead, a new metal gate system has been introduced to avoid any loss of active area, which otherwise would be rather significant. This system not only reduces the internal gate resistance but also enhances the gate resistance uniformity across the chip.[4] Furthermore, the field plates are directly connected to the source metal, ensuring a rapid and homogeneous transition at turn-on and turn-off. This minimizes switching losses and mitigates the risk of an undesired dv/dt-induced parasitic turn-on of the MOSFET.

BOOSTING END-TO-END CONVERSION EFFICIENCY IN TELECOM AND DATA CENTER SYSTEMS

Intermediate bus converters (IBCs) are considered a demanding application for power MOSFETs. As part of the intermediate bus architecture (IBA), the IBC is a ***DC/DC converter*** that performs an intermediate conversion to supply the downstream ***point-of-load (PoL) step-down converters***, as shown in Figure 3.

This architecture is prevalent in ***telecom*** and ***data centers*** and aims to achieve the best conversion efficiency from the AC/DC power supply unit to the

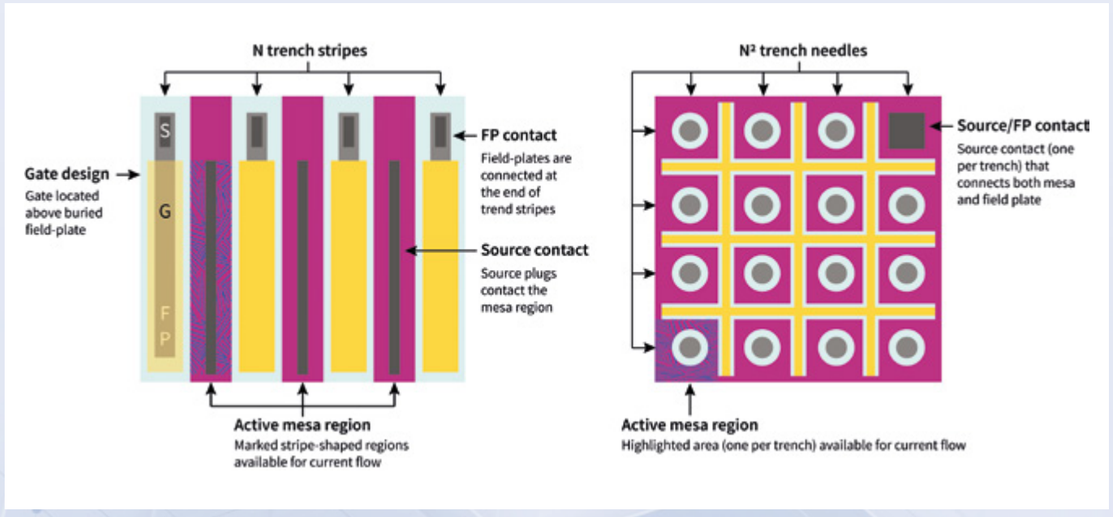

Figure 2: Comparison of the commonly used stripe layout with the new grid-like layout approach

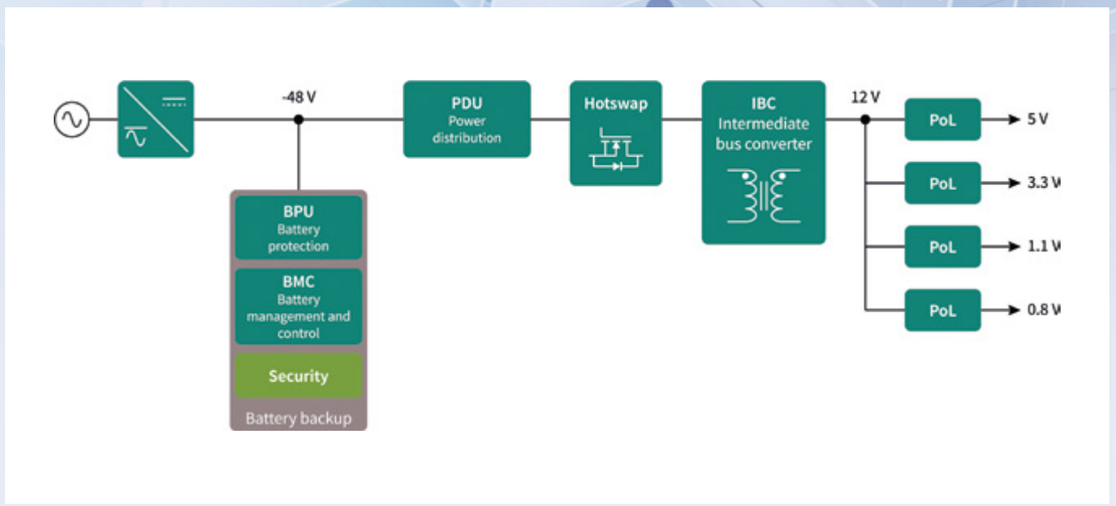

Figure 3: System diagram of the IBA

digital loads (xPUs and ASICs).[5] Depending on the end application, PoL converters can be optimized to operate either with a narrow or wide input voltage range.
In telecom systems, where the –48-V bus shows wide tolerance, it has been common for the PoL regulators to operate with a narrow input voltage range (e.g., 12 V), thus requiring a regulated IBC. Taking the burden of the regulation from a wide input range (–36 V to –75 V), the IBC tends to be rather inefficient and plays an important role in defining the end-to-end conversion efficiency. Improving the IBC efficiency is thus paramount to boosting the overall conversion efficiency.

In ***modern data center systems*** or ***advanced AI hardware accelerators***, extremely high currents have to be supplied to sub-1-V digital loads. The efficiency of the two stages can be maximized by playing with the down-conversion ratio of the IBC and with the burden of regulation being transferred to the multiphase PoL/voltage regulator module. Indeed, unregulated IBCs in the form of DC transformers (DCX) are employed in these applications, showing typical peak efficiencies that exceed 98%, much higher than their regulated counterparts.

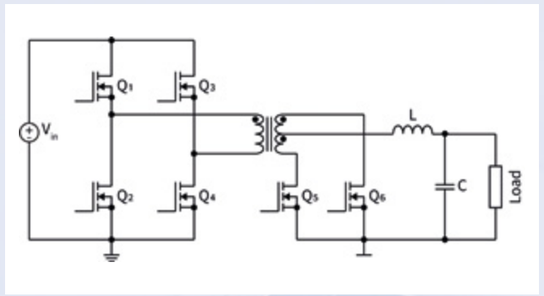

Figure 4: Simplified schematic of the 600-W IBC board in FB-CT configuration

DEVICE BEHAVIOR AND EFFICIENCY MEASUREMENTS UNDER HARD-SWITCHING CONDITIONS: TESTING A 600-W IBC FOR TELECOM APPLICATIONS

The IBC in this application operates as an isolated DC/DC IBC with a nominal –48-V input (overall range from –36 V to –75 V) and a 12-V output voltage bus. The fully regulated converter in the industry's standard quarter-brick form factor operates at a switching frequency of 250 kHz and can deliver an output current of a maximum of 50 A. The IBC is based on a hard-switching full-bridge (FB) topology with a center-tapped (CT) synchronous rectifier (SR) on the secondary side, schematically shown in Figure 4.

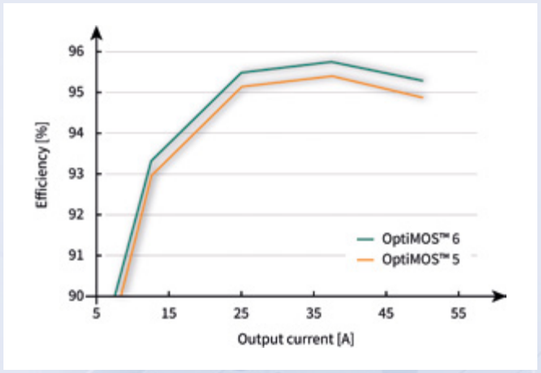

Figure 5: Efficiency in the 600-W IBC comparing the new and predecessor technology

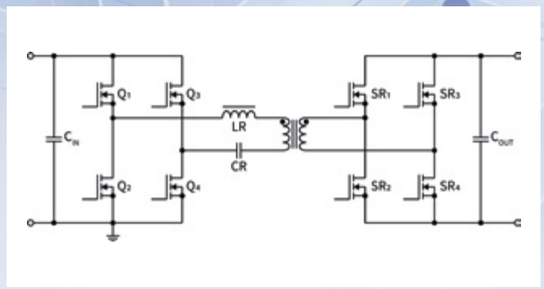

Figure 6: Schematic of the 1-kW IBC board with an FB LLC on the primary side

The primary side uses Infineon's latest trench MOSFET technology, OptiMOS™ 6, employing 100-V devices (***ISC030N10NM6***) with $R_{DS(on),max}$ = 3.0 mΩ. These devices come in a SuperSO8 package (PQFN 5 × 6 mm²) and replace the ***BSC050N10NS5*** from the predecessor OptiMOS™ 5 technology, which had a higher $R_{DS(on),max}$ of 5.0 mΩ (also coming in a SuperSO8 package). On the secondary side, the system uses 80-V MOSFETs as SRs. It utilizes either four paralleled ***OptiMOS™ 5 BSC040N08NS5*** devices with $R_{DS(on),max}$ = 4 mΩ and a SuperSO8 package from the predecessor technology, or four paralleled OptiMOS™ 6 ISZ053N08NM6 devices[i] with the industry's lowest $R_{DS(on),max}$ of 5.3 mΩ and a smaller PQFN 3.3 × 3.3-mm² package.

The results obtained from the comparison of measured efficiencies, presented in Figure 5, highlight the advantages of adopting OptiMOS™ 6 technology. Compared with the previous generation, the solution employing OptiMOS™ 6 technology demonstrates impressive efficiency improvements in excess of 0.4% from 20% load up to full load. Using a smaller package footprint reduces the PCB area allocated for SR devices by up to 64%. Additionally, the maximum temperature at the hotspot of the converter on the primary side decreases by 7.5°C.

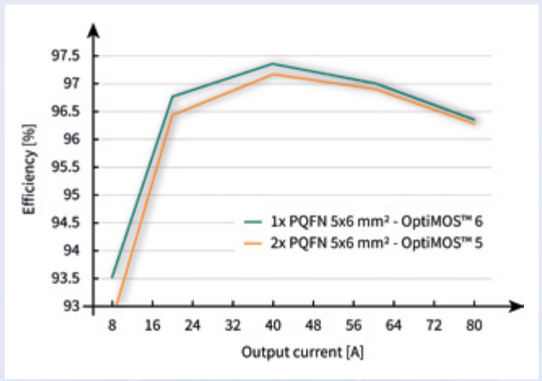

Figure 7: Efficiency in the 1-kW LLC IBC comparing the new and predecessor technology

EFFICIENCY MEASUREMENTS UNDER SOFT-SWITCHING CONDITIONS: TESTING A 1-KW IBC FOR DATA CENTERS

This 1-kW, 4:1, fixed-frequency LLC IBC operates as a DCX from an input that may vary from 42 V to 60 V. The soft-switching techniques employed in the LLC resonant topology allow a significant efficiency improvement in ***telecom*** and ***server power supplies***.[6–8]

In Figure 6, two OptiMOS™ 6 80-V power MOSFETs housed in a SuperSO8 package are paralleled on the primary-side FB. An FB configuration is formed using four ***OptiMOS™ 5 25-V IQE006NE2LM5*** source-down devices (PQFN 3.3 × 3.3 mm²) in parallel as SRs. The turns ratio of the transformer is 4:1. The resonant frequency of the LLC converter is 310 kHz. The switching frequency is fixed to match the resonance frequency of the tank. Zero-voltage switching for the primary switches and zero-voltage/zero-current switching for the SR switches are thus achieved by design.

The significantly improved device parameters of the new OptiMOS™ 6 80 V not only improve the overall efficiency of the converter but also allow the two paralleled ***SuperSO8 OptiMOS™ 5 80-V power MOSFETs BSC030N08NS5*** with $R_{DS(on),max}$ = 3 mΩ on the primary side to be replaced by just one OptiMOS™ 6 ISC014N08NM6 device,[i] with the industry's lowest $R_{DS(on)}$ of 1.45 mΩ. Figure 7 compares the efficiency for this case, revealing an improvement over the full load range, with up to 0.8% better values using the latest device technology. Additionally, the single device of the new generation remains even cooler than if two devices from the previous generation are used.

CONCLUSION

This article discusses Infineon's latest OptiMOS™ 6 trench MOSFET technology, featuring the new 80-V and 100-V power MOSFET devices.
The new OptiMOS™ 6 devices surpass their predecessors in all critical parameters, offering a combination of low on-state resistance and superior switching performance. With a focus on high-switching–frequency applications like ***telecom SMPS*** and ***solar energy systems***, this technology holds immense potential for bringing significant improvements to various other application fields.

i This product will launch soon. For engineering samples, click here to place a request.

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COVER STORY – DESIGN

The advances in overall device performance are remarkable, resulting from significant improvements at a device technology level. These improvements led to the creation of a unique device structure, the first to employ a 3D charge compensation in conjunction with a metal gate in a trench power MOSFET. As a result, this technology reduces on-resistance, dramatically lowers gate- and gate-drain charges and improves the switching homogeneity across the device area. These achievements translate into a significant enhancement in system efficiency in various applications across different load conditions.

The efficiency measurements carried out on several SMPS applications under both hard- and soft-switching conditions confirm the remarkable findings at the semiconductor device level. Depending on the topology and load condition, it is possible to raise efficiency by up to 1%, further highlighting the superiority of this new technology. Additionally, the much-improved device performance reduces the number of devices required by up to 50% without any adverse effect on the device temperature, demonstrating its potential to significantly lower costs and improve overall system reliability.

To learn more about the latest power MOSFET technology family and its potential to revolutionize the telecom power arena and other application fields, we encourage you to visit our ***webpage***.

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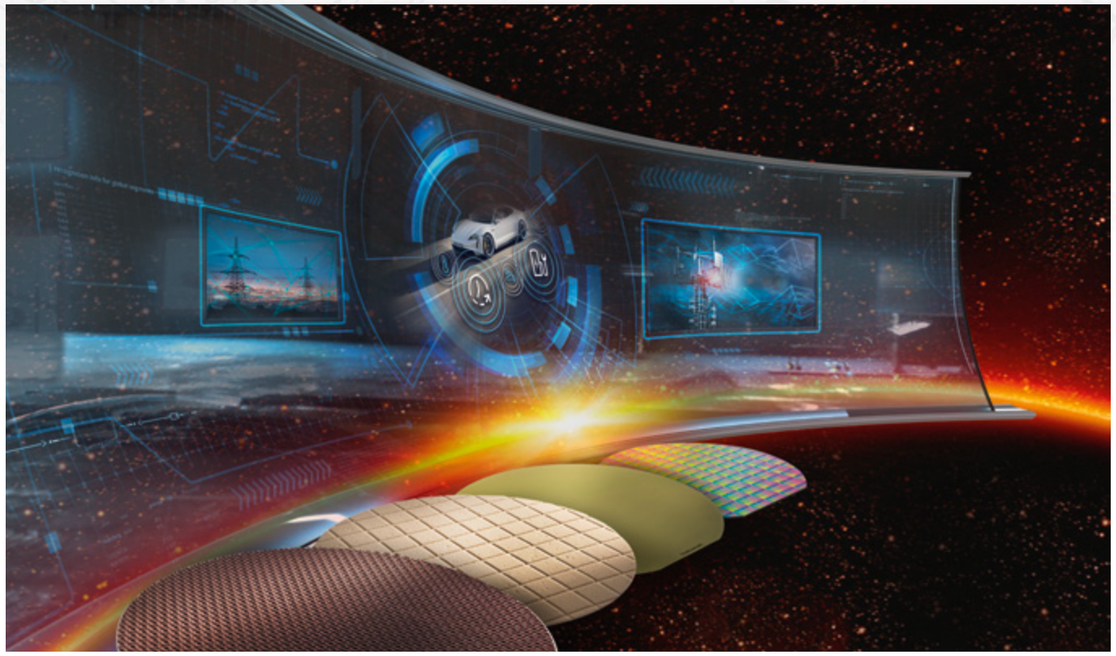

Slicing and Surface-Finishing Solutions for SiC Wafering

By Maurizio Di Paolo Emilio, editor-in-chief of Power Electronics News

Today, silicon carbide is used in demanding semiconductor applications like trains, turbines, electric vehicles and smart grids. Due to its physical and electrical properties, SiC-based devices are suitable for applications in which high temperature, high power density and high operating frequency are common requirements. Although SiC power devices enable advancements in demanding sectors like EVs, 5G and IoT technologies, the production of high-quality SiC substrates offers multiple challenges to wafer manufacturers.

Amazingly, the biggest potential is still in front of us. SiC-based semiconductors, which serve as the foundation of technology, will continue to enable significant advancements in a variety of fields, including automotive, consumer electronics, aerospace and medicine. Currently, automotive applications dominate the SiC market and make up more than 75% of the total power SiC device market. The accelerating adoption of SiC results in a CAGR of 34% in the forecast period of 2021–2027.

SiC APPLICATIONS

SiC is the chosen substrate material for advanced semiconductors, particularly for power electronics, to manage the growing demands of electronic devices. It allows 15× greater breakdown voltages, a 10× stronger dielectric breakdown field and a 3× stronger thermal conductivity. Additionally, SiC has a 2× to 3× higher current density and allows for higher operating temperatures (up to 400°C, versus 150°C for silicon).

SiC semiconductors are in higher demand across a variety of industries due to its performance at high temperatures, voltages and power levels. SiC power supplies, for instance, are used in data centers to significantly reduce the amount of power needed for cooling systems. Uninterruptible power supply systems also guarantee a constant, reliable source of power. Another application is the augmented power needs of 5G base stations, which handle an increasing amount of data. SiC semiconductors provide higher power at a smaller size and are used for megahertz switching.

BENEFITS FOR THE AUTOMOTIVE INDUSTRY

The automotive industry benefits from the advantages of SiC in the following applications:

- On-board battery charger: In this application, SiC can double the power while halving the size.
- On-board DC/DC converter: SiC is used to convert the on-board battery voltage into a clean 12-VDC bus to power on-board equipment.
- Powertrain: Here, SiC helps to reduce switching losses to less than 80%, with 30% smaller size. This results in a smaller battery (less weight, less heat) and longer range.
- Off-board DC fast-charging stations

The industry's biggest hurdle will come from not only the sheer volume of wafers needed to meet demand over the next five years but from modifying wafer parameters to match those of silicon wafers. Current and next-generation production techniques will be pushed by tighter tolerances and standards. To overcome these obstacles, innovation will be essential.

PUREON'S SOLUTIONS FOR SiC MANUFACTURING

Because the market aims for power device price parity with Si-based devices, SiC substrate producers are motivated to increase process efficiency and lower wafer-production costs. Additionally, SiC-based applications and all other types of semiconductors are in extremely high demand, necessitating innovation in the manufacturing process.

Most manufacturers believe that reducing process times or using less expensive consumables will save costs. However, a large reduction in cost of ownership will be attained by an increase in yield. The entire manufacturing process is impacted by consumables and surface-finishing options. In this effort to optimize yields, the uniformity of pads, slurries and templates from run to run and lot to lot is essential. The two decades of product development for the SiC market and Pureon's semiconductor experience help the company overcome manufacturing obstacles.

SOLUTIONS THAT OPTIMIZE AND BOOST YIELDS

Pureon performs testing and produces data with its own polishing and surface laboratories because it is a manufacturer of consumables with internal wafer-processing capabilities. This feature offers customers representative data to reduce risk in the testing and qualification of new products, as well as dramatically reduced development cycle times for Pureon. The testing and acceptance processes are sped up at the wafer makers' facilities as a result.

Wafers that are 200 mm in diameter require entirely new manufacturing processes and machinery. New manufacturing technologies are being introduced at every stage of the process to create high-volume manufacturing processes for these new requirements. Pureon is ideally positioned to offer SiC wafer producers next-generation solutions, enabling the market's maturing by increasing productivity and lowering cost of ownership. With shorter cycle times and longer consumable lifetime, Pureon's solutions optimize and boost yields.

WHERE PUREON'S SOLUTIONS ARE USED

Wafer blanks from the single crystal or ingot must first be cut to prepare SiC substrates for device manufacture. The main method for accomplishing this is by precisely cutting wafer blanks from the SiC ingot using a multi-wire saw with a thin wire operating at high speeds in conjunction with a diamond abrasive slurry. Figure 1 shows the general process flow for the manufacture of SiC wafers.

In the process of making wafers, cutting high-quality blanks successfully at the wire-saw step is likely the most crucial step because wafer-shape enhancements at a later stage are very challenging to improve. When it comes to the wire-saw process, Pureon offers both oil-based and non-oil-based diamond abrasive slurry as options. To further improve this process, Pureon works closely with both wire-saw OEMs and customers. The slurries' proprietary chemistry and categorized diamonds ensure lot-to-lot uniformity, which leads to repeatable processes at the customers' sites and increases wafer yield and quality.

HIGH SURFACE QUALITIES AND IMPRESSIVE STOCK REMOVAL RATES

The mechanical polishing of the wafers using a polishing slurry including diamonds and a polishing pad is the next significant step in the production of SiC substrates. On double-sided, single-sided or a combination of double- and single-sided polishing tools, typical processes are carried out. The result of

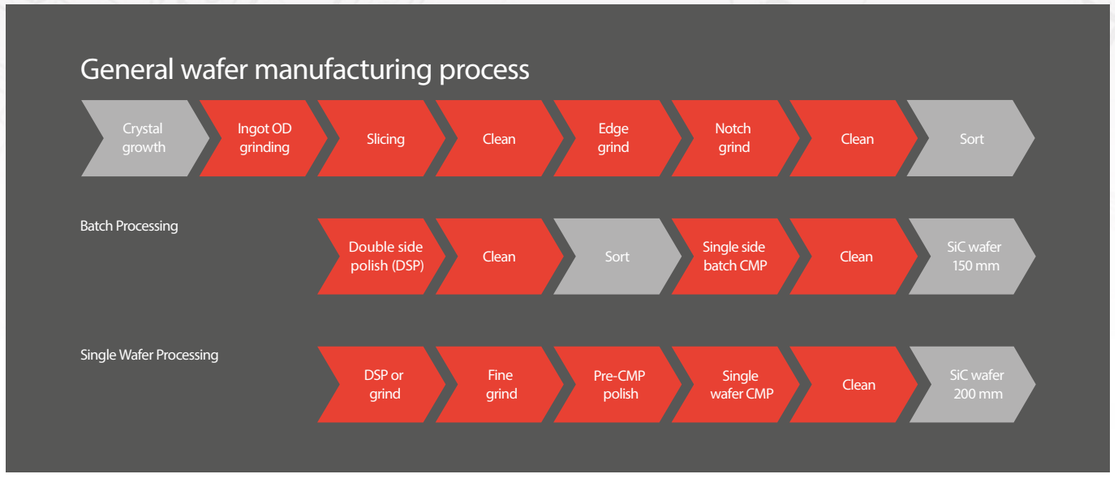

Figure 1: Manufacturing SiC wafers (Source: Pureon)

this production step is a wafer that is extremely flat and has a low level of roughness when it is ready for final polishing.

The creation of diamond-based slurries has long been a top priority for Pureon's innovation team. The business has found highly optimized formulations that let material removal rates on the various SiC substrate faces be modulated. Pureon has developed new solutions for lapping SiC wafers, which allows for high surface qualities and impressive stock removal rates at the same time.

BETTER RESULTS WITH CMP POLISHING PADS

Chemical mechanical polishing (CMP) is the name for the last significant stage in the manufacture of SiC wafers. This process step has the sole purpose of preparing the substrate surface for epitaxial growth, with no or little wafer-shape modification. This is normally accomplished by removing only a few microns from the wafer surface using a highly reactive chemical polishing slurry and a polyurethane-based or urethane-impregnated felt-type polishing pad. In single-side batch tools, wafers are transported to the polishing pad and secured using a template.
In single-wafer tools, wafers are secured using a vacuum chuck and a backing film. These wafer carriers' materials must have strong resistance to the highly reactive chemistry of the polishing slurry, as they are exposed to it.

To improve cost of ownership and increase service life, Pureon keeps creating cutting-edge wafer templates and films for use in this process. Two new polishing pads for SiC CMP have been released to the market thanks to tight collaboration between Pureon and the industry. The CMP procedure is now more productive and produces better results thanks to these new CMP polishing pads.

CONCLUSION

Significant improvements in substrate production, both in its current form and in the creation of next-generation substrates, are necessary to support the expansion of the SiC device market. For nearly 20 years, Pureon has provided the SiC wafering sector with support through its knowledge, products and expertise in this space. Pureon's specialists keep coming up with new ideas, increasing substrate yields and bringing down the price of SiC wafers, allowing this technology to be used more quickly.

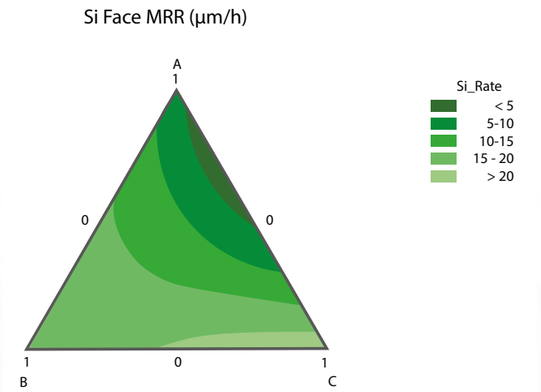

Figure 2: Representative silicon face MRR (µm/hour) response surface in a three-component mixture design using 3-µm monocrystalline diamond (Source: Pureon)

Power Electronics and Energy Storage in Grid Modernization

By Sonu Daryanani, contributing writer for Power Electronics News

As the world shifts to increased use of renewable energy, a transformation is occurring in the storage and conversion of this energy for everyday household use. In this article, we will highlight a presentation[1] delivered by Jacob Mueller, a senior member of the technical staff with the energy storage technology and systems department at Sandia National Laboratories, on the key trends and challenges involved in this transformation, focusing on the role of power electronics and energy storage.

GRID ENERGY STORAGE

A bidirectional electrical energy storage system is capable of absorbing the energy and storing it for a period of time before sending it in the form of electricity. It can come in many forms, as shown in Figure 1. Variable ***renewable energies*** like wind and solar are driving the growth of battery storage systems. A distributed approach (termed DER, for distributed energy resource) using smaller batteries at the source of generation can make the grid flexible and reliable. Current battery technology is mostly applicable to short-duration energy storage, in the range of seconds to hours. Pumped hydro, compressed air and thermal methods offer hours to daylong storage but can often be limited by natural resources and terrain.

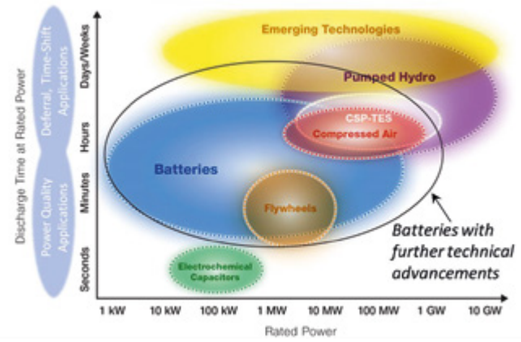

Figure 1: Energy storage techniques versus power and discharge time (Source: U.S. Department of Energy, "Potential Benefits of High-Power, High-Capacity Batteries," January 2020)

As Figure 1 shows, there is no ready solution for seasonal long-duration energy storage.

Lithium-ion battery energy storage systems (BESS) are dominant within battery storage technologies. Examples of large-scale installations include the AES

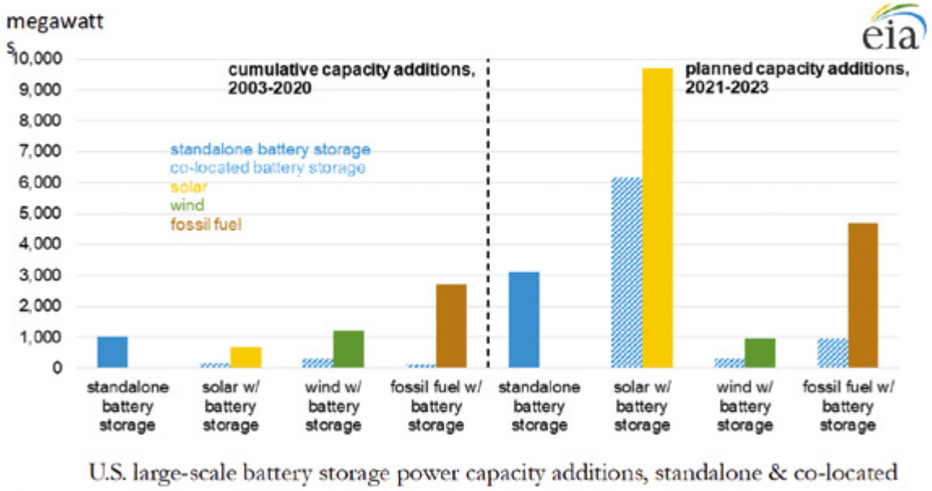

Figure 2: U.S. large-scale battery storage additions (Source: U.S. Energy Information Administration, "Battery Storage in the United States: An Update on Market Trends," December 2020)

120-MWh BESS in Escondido, California, and the Tesla 129-MWh system in Australia. Figure 2 shows the U.S. large-scale battery capacity addition, for the time periods from 2003 to 2020 and 2021 to 2023. This shows the acceleration in both standalone and co-located storage systems.

While the price of batteries is coming down significantly, as shown in Figure 3, the overall BESS cost includes several other components, such as the power conversion system, which includes a bidirectional inverter, an energy management system that provides safety and data-logging controls and other components like the container, electrical distributions and HVAC/thermal management.

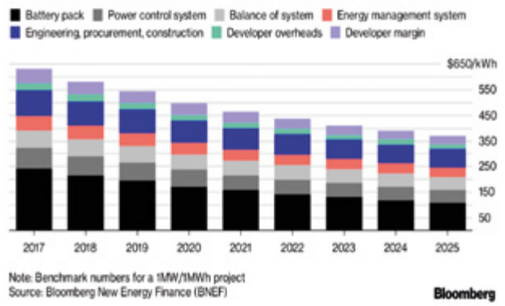

Figure 3: Price trend of BESS (Source: Bloomberg New Energy Finance)

POWER ELECTRONICS SYSTEMS

Power electronics systems (PES) provide two critical functions within the grid:

- Convert energy efficiently between different types, e.g., DC to AC
- Control the flow of electrical energy

As shown in Figure 4, a PES is needed from energy generation, transmission to its distribution.

In the U.S., the Office of Electricity's Transformer Resilience and Advanced Components (TRAC) program highlights the future roadmap in various aspects of energy generation and distribution. One aspect of this covers the solid-state power substation (SSPS). An SSPS power converter within the substation can be constructed as a modular collection of power electronics building blocks. Scalability is a key end goal. The SSPS roadmap, shown in Figure 5, highlights the trend to increased power density going from SSPS 1.0 to SSPS 3.0.

Increasing the working voltage is one of the best routes to increasing power density. A battery-cell voltage is fixed by the cell chemistry. Hence, several cells are stacked in a series combination to create modules, which can then be series-connected to create a rack. Racks can then be parallel-connected for capacity to create an individual system. A power control system (PCS) controls this system and presents a voltage to the DC-link.

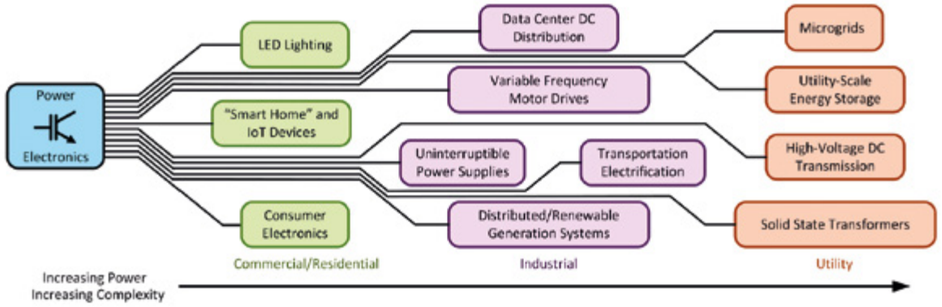

Figure 4: Role of power electronics systems in energy storage and distribution[1]

2020 DOE/OE TRAC Program Solid State Power Substation Roadmap

		SSPS 1.0 UP TO 34.5 KV UP TO 10 MVA	SSPS 2.0 UP TO 138 KV UP TO 100 MVA	SSPS 3.0 ALL VOLTAGES ALL POWER LEVELS
GOALS	**R&D Challenges**	**Goals**		
SUBSTATION APPLICATION	Converter System Cost and Performance	< $150/kVA > 96% 2 MW/m³ 10-Year Mean-Time-to-Failure (MTTF)	< $125/kVA > 96.5% 5 MW/m³ 20-Year MTTF	< $100/kVA > 97% 10 MW/m³ 40-Year MTTF
CONVERTER BUILDING BLOCK	Block/Module Cost and Performance	< $20/kVA > 97% 5 W/cm³ 2-Year MTTF	< $15/kVA > 98% 10 W/cm³ 4-Year MTTF	< $10/kVA > 99% 20 W/cm³ 8-Year MTTF
	Drivers and Power Semiconductors	≥ 1.7 kV $0.10/kW	≥ 3.3 kV $0.10/kW	≥ 10 kV $0.10/kW
	Dielectric, Magnetic, and Passive Components	160 kV/mm 0.1 H/m 6.0x10⁷ S/m	600 kV/mm 1.0 H/m 1x10⁸ S/m	2000 kV/mm 2.0 H/m 1.5x10⁸ S/m
	Packaging and Thermal Management	> 500 W/(m²°C)	> 1000 W/(m²°C)	> 10,000 W/(m²°C)

Figure 5: 2020 DOE/OE TRAC program solid state power substation roadmap (Source: U.S. Department of Energy 2020 TRAC report)

Increasing the working voltage is one of the best routes to increasing power density. A battery-cell voltage is fixed by the cell chemistry. Hence, several cells are stacked in a series combination to create modules, which can then be series-connected to create a rack. Racks can then be parallel-connected for capacity to create an individual system. A power control system (PCS) controls this system and presents a voltage to the DC-link.

A conventional PCS solution typically consists of a single-stage inverter, shown in Figure 6.

In this case, the DC-link voltage sets the constraint, as it needs to be greater than the peak AC voltage with some margin. Although this single-stage PCS is cheap, it suffers from disadvantages of lack of scalability. Within series-connected battery cells, there is variation in cell voltage and current, and this also changes with

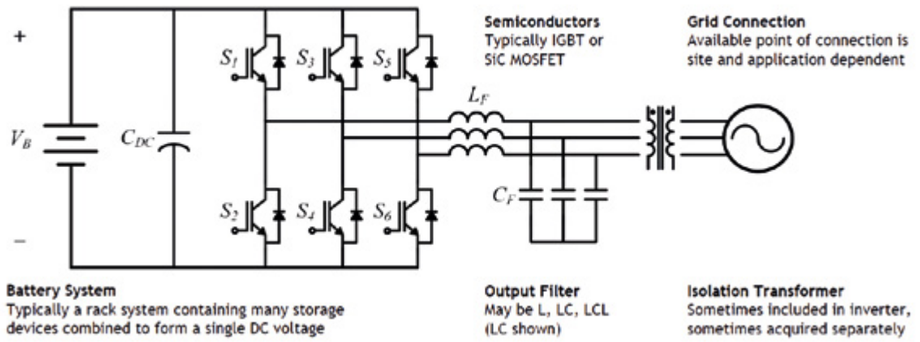

Figure 6: Conventional single-stage PCS[1] (Source: Muller)

aging. The weakest cell can be a fail path for a system and can be a reliability bottleneck. Hence, this simple single-stage PCS is used only for 600-V voltages or lower.

A multi-stage PCS, shown in Figure 7, offers advantages of breaking the DC-link voltage constraint. Some advantages of a multi-stage PCS[2] are:

- Higher voltages in the first stage, which can leverage the benefits of higher-voltage SiC devices and multi-level inverter topologies
- Improved DC voltage stability, allowing for a reduced DC-link capacitor and improved lifetime

Some disadvantages of the multi-stage approach include higher costs, as well as increased power conversion loss.

Multi-level inverters within each stage are commonly used. These have several advantages[3] over traditional two-level inverters, including:

- Reduced harmonic distortion
- Lower switching losses
- Lower PWM switching frequency
- Increased power rating
- Ability to use lower-voltage–rated devices for a higher-voltage application

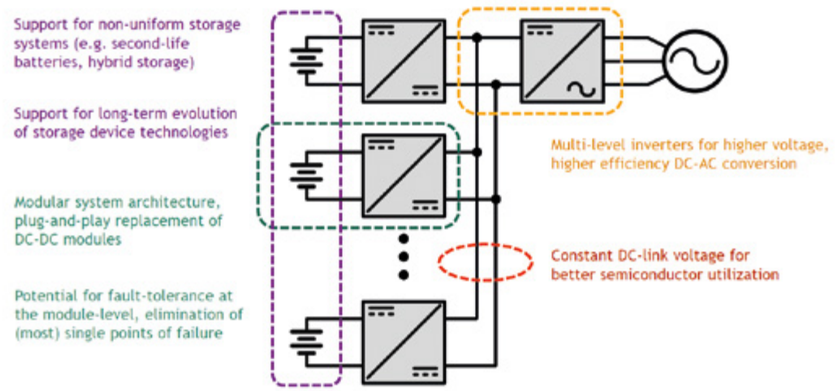

Figure 7: Multi-stage PCS[1] (Source: Muller)

Modularization for improved reliability can come in several ways. Figure 8 shows a parallel PCS. The modules in each parallel leg can be hot-swappable storage/converter modules, and the battery parameters within each leg do not have to be well-matched. The scalability here is still limited by the voltage gain within each of the DC/DC converter stages.

A series-connected PCS is depicted in Figure 9. This has advantages of creating a higher DC-link voltage, enabling reduced conduction losses from cabling. This architecture is more forgiving for even modest gain in DC/DC converters.

CONCLUSION

SiC-based power electronics are helping revolutionize both storage and grid distribution systems, making the use of distributed, renewable energy generation much more practical. Key bottlenecks still remain, particularly in long-duration energy storage, the manufacturing of large-storage–capacity Li-ion batteries and passive components like magnetics that go into the PCS stages.

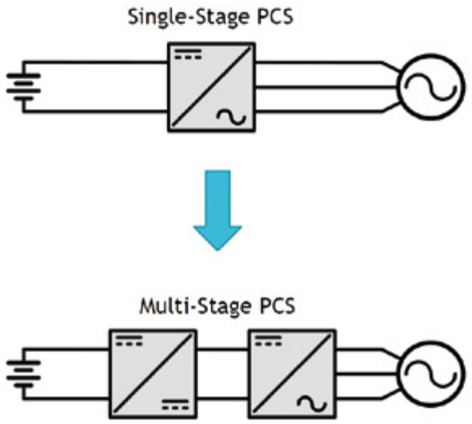

Figure 8: A parallel PCS[1] (Source: Muller)

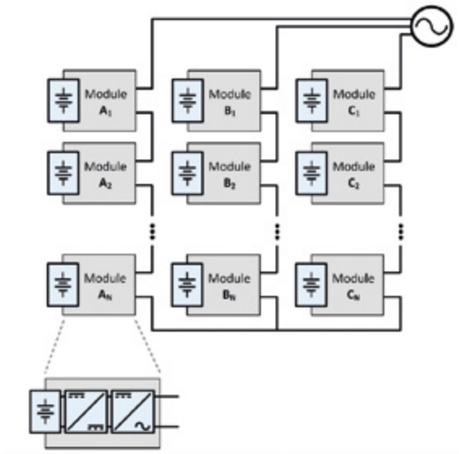

Figure 9: A cascaded, series-connected PCS[1] (Source: Muller)

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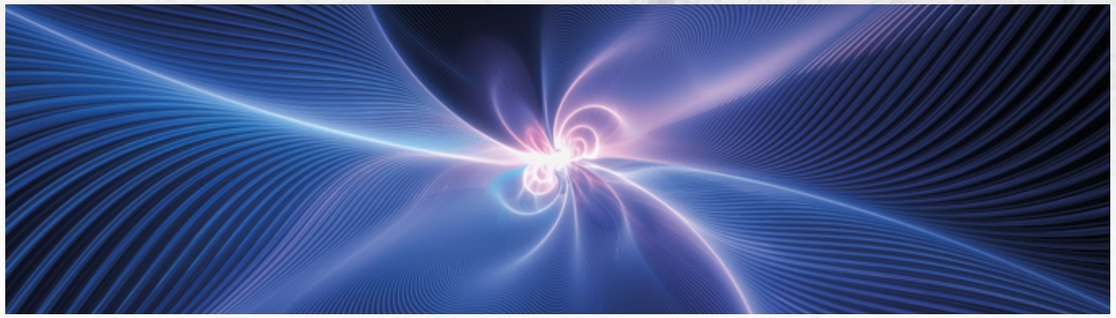
- [1]Mueller, J. (2021). *"Enabling Energy Storage for Grid Applications Through Advanced Power Electronics."* IEEE Energy Conversion Congress and Exposition.
- [2]Zhu, Y., Yao, J., & Wu, D. (2011). "Comparative study of two stages and single stage topologies for grid-tie photovoltaic generation by PSCAD/EMTDC." Proceedings of the 2011 International Conference on Advanced Power System Automation and Protection.
- [3]Salem et al. (2022). *"A Comprehensive Review on Multilevel Inverters for Grid-Tied System Applications."* Energies 2022.



Enabling Clean Nuclear Fuel

How fusion could help play a role in solving the global issue of nuclear waste

By Greg Piefer, CEO and founder of Shine Technologies.

National support for nuclear energy in the United States is the highest it has been in years. A 2022 survey by ecoAmerica showed that more than 61% of Americans believed "a lot more" or "more" money should be spent on next-generation nuclear technology. Climate change, geopolitical challenges and rising energy costs are among the factors in the changing sentiment.

And yet the same barriers to nuclear power that have existed for decades continue to persist today. In the same survey, the two largest public concerns to upgrading nuclear technology were waste disposal and health/safety.

The buildup of spent nuclear fuel continues to be a significant issue both socially and economically. The International Atomic Energy Agency reports nearly 400,000 tons of spent fuel were generated between 1954 and 2016. The United States currently has an estimated 86,000 metric tons of spent nuclear fuel, a number that is growing by about 2,000 tons per year. There are currently just two acceptable storage methods for that spent fuel—either in specially designed pools or in dry cask storage—onsite at reactors across the country.

RECYCLING RADIOACTIVE WASTE

Spent nuclear fuel isn't actually "spent" at all; it still has more than 90% of its energy capacity available. If it could be recycled, it can be reused—again and again—in the same reactors where it originated.

Imagine how much better the public response to nuclear waste would be if we made it clear that instead of creating new waste, we'd be using old waste to refuel our reactors again and again.

With economic, security and climate matters in mind, ***35 members of Congress in November penned a letter to Jennifer Granholm***, the United States Secretary of Energy. They asked the Department of Energy (DOE) to accelerate development of technologies that may increase sustainability of the U.S. nuclear fuel cycle through recycling. They asked the DOE to report on its work to advance technologies that might be used to reduce fuel security risks, be economically viable and help manage nuclear waste produced by the U.S. reactor fleet.

Nuclear and fusion technology companies can play a role in the future in both recycling spent nuclear fuel so that it can be reused and transforming long-lived radioactive waste into shorter-lived materials.

FUSION MAY DRAMATICALLY ALTER LONG-LIVED ISOTOPES

Computers were once expensive machines that took up entire rooms or buildings and were used only in niche applications. But the technology provided

value, which then justified reinvestment. Eventually, computers were a mainstay in offices, then in homes, and now they are so effective and efficient that we carry them in our pockets or handbags.

This is just one example of the process that has been used to commercialize big ideas. And while many private companies are set on making the giant leap to commercializing fusion energy in one bound, others are determined to get there by scaling capabilities and cost economics, which create value along the way.

For instance, fusion technology can be leveraged today to produce vital medicine—including potentially revolutionary cancer treatments—and to examine roads, bridges and critical industrial parts for defects.

Other applications for fusion are coming, including the potential to recycle nuclear waste—the radioactive material leftover after it has been used in a fission reactor, typically at a nuclear power plant.

Fusion companies in the nuclear medicine space are gaining experience in separating valuable materials out of a radioactive stream. It is a process that could be vital to separating fuel from waste so that the fuel can be recycled back to reactors.

Additionally, fusion could play a role in mitigating the leftover long-lived radioactive waste that makes up ~2% of the remaining waste stream after recycling but which creates the requirement for impossibly long-lived repositories. Fusion has the potential to take radioisotopes that can take millions of years to decay and transform them into different radioisotopes that decay in years or less.

ADVANCING CLEAN ENERGY ON THE WAY TO FUSION POWER

Until fusion energy becomes possible, nuclear fission offers a carbon-free source of clean energy to reduce dependence on fossil fuels and help combat climate change. But the lack of a sustainable, closed-cycle fuel pathway is one of the key inhibitors of its growth.

This drawback could be solved by combining recycling technology with fusion technology. By continuing to scale, fusion technology companies can augment the current momentum in the nuclear space—expanding fission's scope, reach and impact while gaining valuable experience with fusion technology that will one day power our futures.

Loss Distribution Among Paralleled GaN HEMTs

By Saumitra Jagdale, contributing writer for Power Electronics News

Gallium nitride high-electron–mobility transistors (HEMTs) are becoming increasingly popular in the world of electronics due to their superior performance over traditional silicon-based transistors. GaN HEMTs can operate at higher switching frequencies, enabling industries to lower the size of electronics used in the system. The superior thermal performance helps them in high-power applications like powertrains for electric vehicles, transmission lines and motor drives.

GaN HEMTs need to be paralleled in numerous applications to increase power capabilities and operational efficiency. But paralleling them comes with its challenges, such as unbalanced distribution of losses between switches, which can lead to an increase in temperature above safe limits. To parallel any two switches, the drain-to-source resistance ($R_{DS(on)}$) of the switches is accurately matched to ensure equal distribution of load between the switches. Any imbalance can lead to high-frequency oscillations between the switches and in turn their destruction.

In the case of GaN HEMTs, the higher switching frequency compared with silicon MOSFETs poses a greater challenge for researchers in paralleling these switches. Due to their ultra-fast operation, GaN HEMTs are very sensitive to circuitry parasitics, and any imbalance between these switches can lead to a loss of efficiency and increases the chances of damage to the switches. Various research has proved that reliable hard switching-on and switching-off transitions can be realized without slowing down or derating the GaN HEMTs.

Another important parameter while paralleling GaN HEMTs is to ensure accurate loss distribution. This article looks at the types of losses and ways to ensure proper monitoring and analysis of loss distribution in parallel GaN HEMTs. The original article may be read ***here***.

DISTRIBUTION LOSSES IN GaN HEMTs

The methods to measure losses in silicon MOSFETs and IGBTs have been well developed, but with the industry demanding faster and more efficient devices, the focus has now shifted to wide-bandgap devices like GaN. Just like silicon-based devices, the losses in GaN can be divided into two categories: static or conduction losses and switching losses. Although the

categorization is similar, a closer look shows that the distribution losses in the case of GaN are different from those of silicon MOSFETs.

In the case of GaN HEMTs, static or conduction losses include the $R_{DS(on)}$ loss at 25°C, $R_{DS(on)}$ loss from the heating effect, $R_{DS(on)}$ loss from the trapping effect (also known as dynamic $R_{DS(on)}$ loss) and deadtime loss. The switching loss includes turn-on/turn-off V-I overlap loss and E_{qoss} and E_{oss} losses. Another kind of loss observed at very high frequency of operation is the C_{oss} capacitance hysteresis loss, which is considered for a radio-frequency range of applications. The V-I overlap loss is caused by the overlapping of the current and voltage during switching operations. E_{oss} is the capacitance charging loss, i.e., the energy lost in charging the parasitic capacitance of the switch. E_{qoss} is the loss caused due to the capacitor charging current of the opposite switch in a half-bridge configuration of HEMTs.

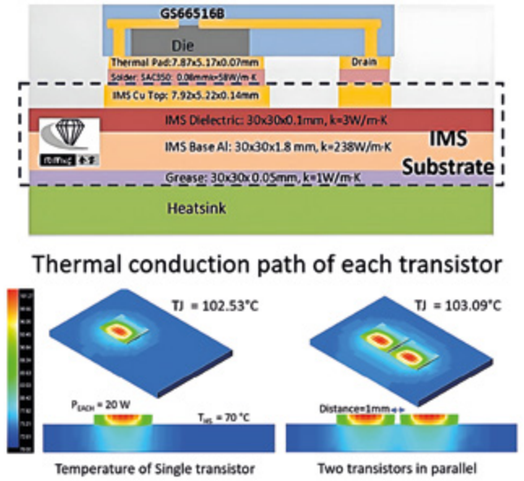
While a significant amount of research has been done on the effect of static losses on the paralleling of HEMTs, this article focuses on evaluating the switching losses that can be as high as static losses in high-voltage and high-frequency applications.

ANALYTICAL MODELS AND EXPERIMENTS FOR ESTIMATING LOSSES

The piecewise linear model is one of the most popular models for analyzing and estimating the losses of a transistor. The model considers the circuit only in terms of the input capacitance and external gate resistor and ignores the parasitic parameters and temperature dependency. Hence, it cannot be used for analyzing the switching losses in a parallel GaN configuration. Many researchers have worked on modifying the piecewise linear model to account for more dynamics in the circuit. To effectively monitor the switching losses, the piecewise linear model has been modified to include parasitic elements and the effects of the synchronous transistors.

To see the effect of temperature on losses, the variation of threshold voltage and transconductance is plotted with a change in the junction temperature of the parallel of the GS66516B GaN HEMT. The threshold voltage was observed to be nearly constant with changes in temperature, but transconductance had a negative dependency on temperature. This results in an automatic junction-temperature–balancing mechanism: When the junction temperature increases, the switching losses decrease considerably. In parallel silicon-based MOSFETs, unlike GaN, the switching losses increase as the junction temperature increases, which can lead to unbalanced temperature distribution or even thermal runaway.

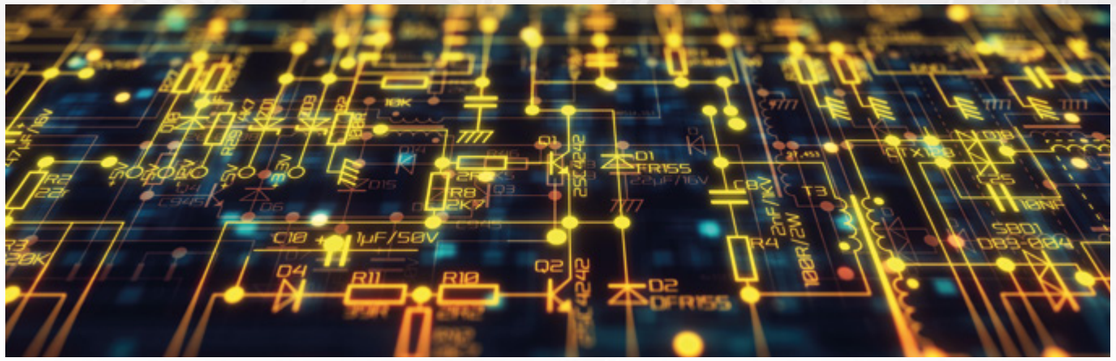
To experimentally verify the above automatic junction-temperature–balancing mechanism, the junction temperature of the parallel GaN HEMTs is measured. The experiment was conducted using a 240-A/650-V half-bridge power module with an IMS substrate built using randomly selected GaN HEMTs. A full power emulation of the circuit at different switching frequencies showed excellent junction-temperature balancing for paralleled GaN HEMTs.



Thermal finite element analysis simulation results of GaN HEMTs on the IMS substrate (Source: IEEE)

Reference

▶ [1]Lu, J., Hou, R., & Chen, D. (2018). ***"Loss Distribution among Paralleled GaN HEMTs."*** **2018 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1914–1919.**



SiC Technology Is Revolutionizing Electrification Trends

By Maurizio Di Paolo Emilio, editor-in-chief of Power Electronics News

While silicon has been the go-to semiconductor material for the devices used in power-electronic converters worldwide for quite some time, the invention of silicon carbide in 1891 brought about an alternative to alleviate the dependency on silicon. SiC is a wide-bandgap (WBG) semiconductor: The energy required to excite an electron into the conduction band is higher, and this wide bandgap has multiple advantages compared with standard Si-based devices.

As a result of having a smaller leakage current and a greater bandgap, a device may operate across a wider temperature range without breaking down or losing efficiency. This has further solidified SiC's importance in the field of power electronics and contributed to a surge in its use, together with the fact that it is chemically inert.

SiC power devices are currently being widely used for applications like power supplies, battery-electric–vehicle (BEV) power conversion for battery charging and traction drives, industrial motor drives and renewable-energy–generation systems like solar and wind power inverters.

The new 1,700-V EliteSiC MOSFET and 1,700-V avalanche-rated EliteSiC Schottky diodes have the goal to provide reliable, high-efficiency operation in energy infrastructure and industrial drive applications. With the 1,700-V EliteSiC MOSFET (NTH4L028N170M1), onsemi delivers higher breakdown-voltage (BV) SiC solutions, required for high-power industrial applications. The two 1,700-V avalanche-rated EliteSiC Schottky diodes (NDSH25170A, NDSH10170A) allow designers to achieve stable high-voltage operation at elevated temperatures while offering high efficiency enabled by SiC.

In an interview with Power Electronics News, Ajay Reddy Sattu, director of product marketing IPS BU at onsemi, noted that there are two key application areas onsemi is focusing on with EliteSiC technology: energy infrastructure and electric vehicles.

According to Sattu, energy infrastructure is the first one where bidirectional power flows to connect large-scale storage systems with commercial or utility-scale solar inverters.

"Bidirectional power flow flexibility means round-trip efficiency is an important metric; as such, even a modest 0.5% improvement in efficiency generally results in a significant amount of energy that would be generated at the utility-scale level," Sattu said. "Let's consider a typical solar application where the DC output voltage is boosted to a 1,100-V DC bus and then inverted to a three-phase AC. Here, in Figure 1, the boost stage can be implemented by using a full-IGBT [Si IGBT + diode] module solution

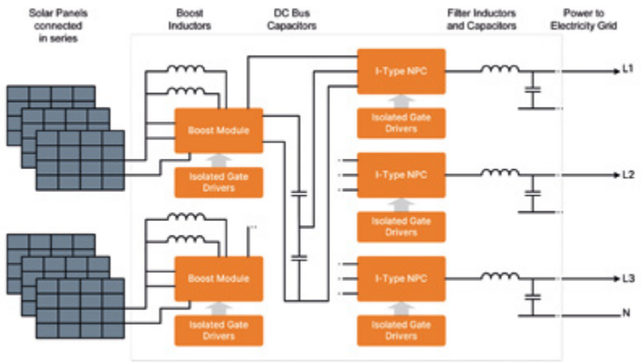


Figure 1: Solar panel application (Source: onsemi)

or a hybrid IGBT [Si IGBT + SiC diode] or a full-SiC [SiC MOSFET + SiC diode] solution. While hybrid solutions have become common already, SiC-based full solutions will challenge them as SiC wafer costs reduce in the coming years. Assume that the system-level conditions are 500 V/25 A, F_{sw} of 16 kHz and output voltage of 800 V with a 600-µH boost inductor."

According to Sattu, from Table 1, comparing a hybrid-IGBT solution and full-SiC solution, it's clear that under the same conditions, overall losses are significantly better in a full-SiC solution, resulting in better efficiency.

"However, with SiC full modules, the switching frequencies can be increased 40 kHz or higher, resulting in the boost inductor to be as low as 200 µH, resulting in lower cost and weight," Sattu said.

Parameter	PIM-IGBT	PIM-SiC
Conduction Loss	13.33 W	12.17 W
Switching Frequency	16 kHz	16 kHz
Turn On Loss E_{on}	3.8 W	3.17 W
Turn Off E_{off}	34.66 W	3.06 W
Total Loss	51.79 W	18.39 W
T_j (T_c = 95°C)	137.9°C	109.9°C

Table 1: Comparing a hybrid-IGBT solution and full-SiC solution (Source: onsemi)

The second key focus area is EV chargers. According to Sattu, the EV chargers of today fall into three main categories, separated mainly by their voltage input and power level.

"Level 1 is typically 120 V AC, is single-phase and typically comes from a household outlet with max current rating of 15–20 A and very slow charge rate," Sattu said. "Level 2 is 220 V AC, is available at home, workplace or public locations and adds 12–80 miles per hour, depending on the power output level. Level 2 chargers can deliver up to 7.7–11 kW, making them capable of charging the average EV in about two to eight hours. The much larger DC quick chargers are Level 3 and only available at commercial locations that have access to three-phase power from their local utility provider. These systems can add up to 100 miles or more of range to an EV battery in just 30 minutes. Let's look at a typical EV charging station block diagram in Figure 2. Let's take the example of a DC fast charger at the system level. On the front end, there is a three-phase power-factor–correction [PFC] boost stage, implemented in a variety of topologies, such as two-level, three-level, uni- or bidirectional. The voltage levels from the grid 400 [EU]/480 [U.S.] are boosted up to 700–1,000 V. A subsequent DC/DC isolated stage converts the bus voltage into the required output voltage. The output voltage aligns with EV battery voltages, typically 400 V or 800 V, and needs to cover the voltage charging profiles. Therefore, the DC/DC output range might swing from 150 V up to 1,500 V. The value proposition of SiC MOSFETs comes into the picture here. To accommodate the bidirectional charge/discharge process and wide voltage range of EV batteries, IGBTs are replaced with SiC MOSFET solutions."

DESIGN CHALLENGES

A number of basic long-term effectiveness concerns based on SiC quality, dependability and supply arise as an increasing number of designers are presently using or have previously used SiC in their designs. With the commercialization and evolution of SiC MOSFETs, gate-oxide reliability has improved significantly as well.

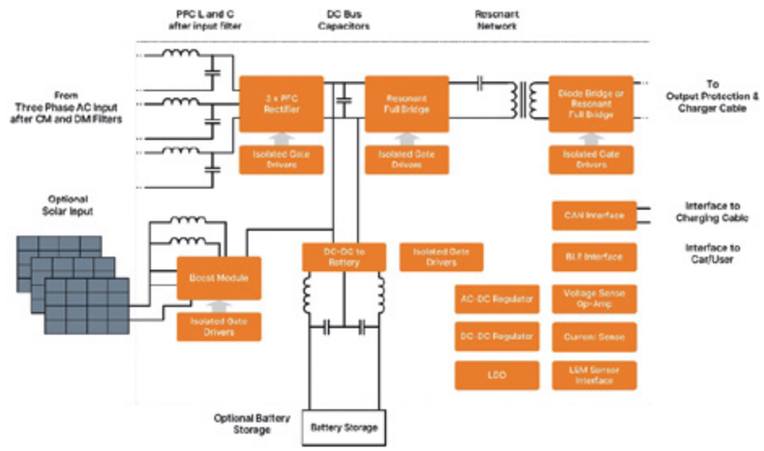


Figure 2: EV charging station block diagram (Source: onsemi)

The gate oxide and ways to shield it from high electric fields remain a key focus area in device development. Improved screening tests are also important to filter out die that may have parametric drifts over time.

The gate-oxide defect density must be kept to a minimum during processing to make SiC MOSFETs as dependable as their Si counterparts. Innovative screening methods must also be created to find and remove possibly weak devices, such as in the electrical end test.

"At onsemi, we consider gate-oxide reliability in numerous ways—intrinsic and extrinsic," Sattu said. "First, our EliteSiC process flow has been robustized to include screening measure at various process steps to screen out possible process-induced failure modes. Second, we also implement either a wafer-level or package-level burn-in methodology to eliminate early-life failures. In addition, as part of an intrinsic reliability study, we evaluate our EliteSiC MOSFET technologies under time-dependent dielectric-breakdown characterization to ensure devices operate beyond what is required from application profiles. Obviously, the tradeoff between oxide thickness and channel mobility limits what oxide thicknesses are used and the V_{GS} (15 V or 18 V) applied in the application, determining the long-term reliability."

Figure 3 compares lifespan performance at V_{GS}, which is substantially greater than what is employed in practical applications. According to Sattu, it is obvious that it would go well beyond any industrial or automotive use cases to obtain appropriate levels of failures under operational settings.

WBG semiconductors have a lot of potential, but designers need to be aware of the difficulties that come with using these materials. It is feasible to accomplish a size reduction of passive components (inductors and capacitors) and to create lighter and smaller systems by operating at greater switching frequencies and at higher power densities. However, it can be challenging to predict how these smaller passive components would behave while operating at higher frequencies, and heat management concerns may occur. Because they function at greater temperatures than those supported by Si-based devices, WBG semiconductors require careful design. Greater thermal stresses are taken into account throughout the design phase, which may negatively impact the system's dependability. Reproducing or simulating harsh working circumstances in which electronic devices are subjected to extreme thermal stress is one of the major problems for electronic designers.

The goal of thermal management is to effectively remove heat from the die and packaging. According to Sattu, there are few avenues to do so.

"First, by implementing a Cu [copper] baseplate option to improve the R_{th} from device junction to the heatsink—this is very crucial, especially for the EliteSiC M3 technology platform, which has the industry-leading specific on-resistance," Sattu said. "As such, the die is small, and by utilizing a Cu baseplate, the effective heat-spreading area will be larger and result in lower thermal resistance. While offering a Cu baseplate is not typical in industrial applications, onsemi offers this option for F5 and Q2 power integrated modules [PIMs]

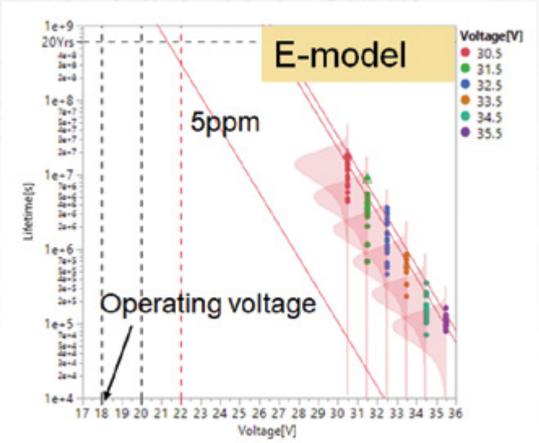


Figure 3: V_{GS} against lifetime performance at V_{GS} much higher than used in real-world applications (Source: onsemi)

and is currently working on developing an F2 module with a Cu baseplate as well. By implementing a Cu baseplate on one of our largest PIMs, F5, R_{thjs} can be improved by 9.3%, as shown in Figure 4. In addition, in applications that will have multiple PIMs on the same PCB board, warpage could be better with Cu baseplate implementation.

"The second improvement comes in the implementation of sintering technologies for SiC devices," Sattu added. "This is already mainstream for automotive products, and in the future, onsemi's industrial products may adopt this die-attach process over traditional solder attach to further reduce thermal resistances."

RENEWABLE ENERGIES

With solar systems ranging from 1,100-V to 1,500-V DC buses, renewable-energy applications are steadily advancing to greater voltages. Customers demand MOSFETs with a higher BV to enable this modification. With a maximum V_{GS} range of –15 V/25 V and suitability for rapid-switching applications in which gate voltages are rising to –10 V, the new 1,700-V EliteSiC MOSFET increases system dependability.

"In the case of utility-scale power plants using a 1,500-V bus, special requirements like low cosmic ray–induced failures, high efficiency and combined with storage functionality will require highly efficient power semiconductors," Sattu said. "We see our SiC MOSFETs and diodes with 2-kV–rated capability will offer performance boost and system cost with 1,500-V DC bus adoption. What will be key here is get to the cost per boost channel or MPPT [maximum power-point tracking] similar to what is being implemented today with Si-based solutions. As SiC manufacturing costs improve, SiC-based 2-kV boost solutions will offer significantly better system costs. Being vertically integrated, onsemi has both the technical and supply chain capability to be a major player in this space."

WHAT'S NEXT?

There are several more applications, besides solar and EV chargers, in which SiC-based devices compete, particularly 650-V–rated devices.

According to Sattu, one such example is in data center power supplies. "With the new 80 Plus titanium requirements and light-load efficiency requirements, there is a system-level shift in how SiC MOSFETs would be used. For example, with the totem-pole PFC implementation on the front end, SiC MOSFETs would be used for the fast leg of the PFC and on the primary side of the DC/DC stage. The key here is not just the performance metric but also to meet the cost metric. Onsemi is currently working on a new 650-V M3 platform to replace the existing Gen 1 platform to further improve benchmark figures of merit and cost position."

Sattu added, "Another emerging application is the industrial motor control market that has stringent requirements for high efficiency and excellent thermal management, low EMI, good controllability and high reliability. Like the energy infrastructure segment, SiC would provide a better value proposition for motor control applications compared with Si IGBTs. For example, in the case of servo drives, for a similar-sized die current rating, pulse current rating would be higher, resulting in passive cooling solutions and the possibility to integrate the drive system with the motor itself. Given that more than 90% of the operation is under constant speed or low torque operation, conduction loss improvement is significant with SiC. Several other emerging applications, such as solid-state circuit breakers, solid-state transformers and fuel-cell inverters, also benefit from similar high efficiency and thermal benefits offered with the EliteSiC portfolio."

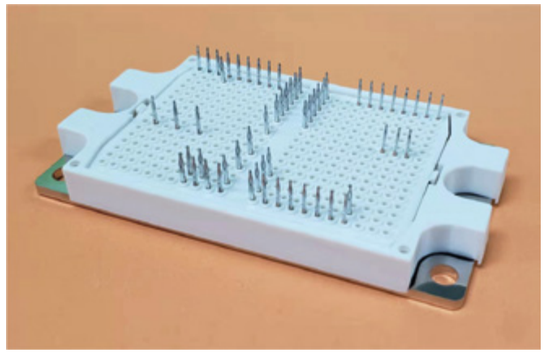


Figure 4: Thermal performance (Source: onsemi)

For e-mobility and renewable-energy systems, power management solutions must provide performance improvements, cost savings and quicker development times. A SiC stack approach that improves performance and lowers prices is currently very advantageous for designers of EVs, commercial transportation, renewable energy and storage systems.

SiC devices are widely used in the automobile industry, notably in the manufacture of EVs and plug-in hybrid vehicles. The power systems for next-generation EVs must be able to boost the vehicle's efficiency (leading to an improvement in range) and the rate of battery recharging.

SiC inverters are proven to be a crucial component of the answer to these problems. An inverter based on SiC can achieve up to 99% efficiency, compared with a standard inverter's 97% to 98% efficiency in transferring energy from the battery to the motor. It is crucial to emphasize how a one- or two-decimal–place boost in efficiency has a big positive impact on the overall vehicle.

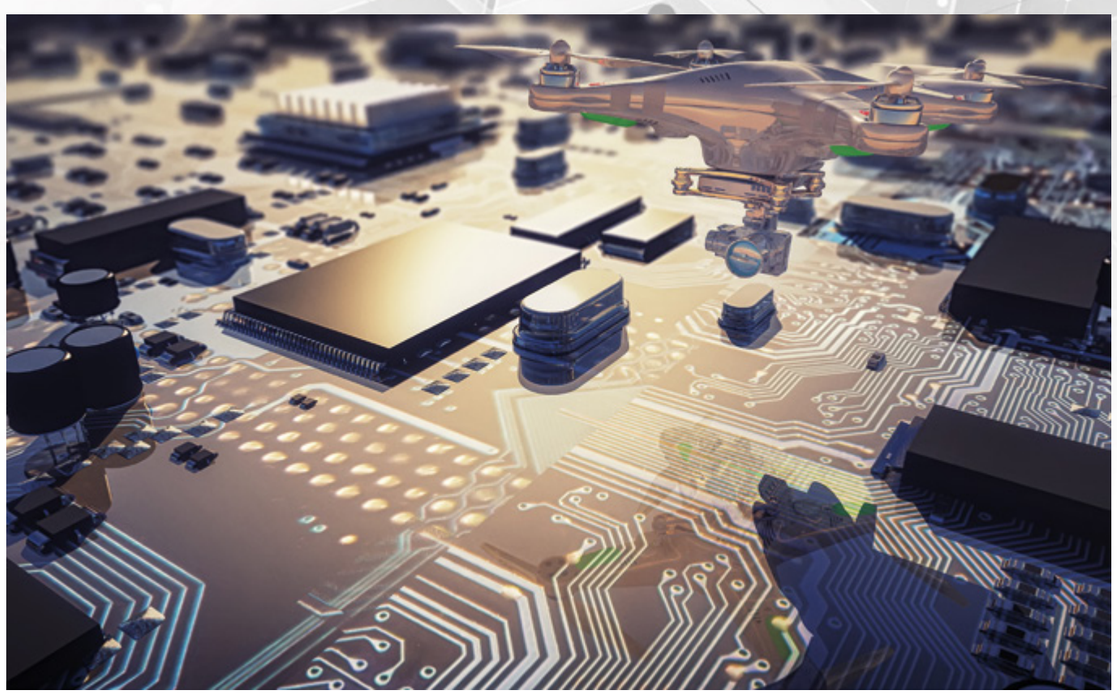
Microgrids have become more important in the effort to reduce greenhouse gas emissions and the amount of energy obtained from fossil fuels due to the rising demand for energy and the expanding usage of renewable-energy sources. However, the microgrid system cannot employ Si-based solid-state inverters and switches because they are too big and ineffective. Due to their greater BV and switching frequency, WBG semiconductors like SiC are positioning themselves as a key element in the development of effective and dependable microgrids.

Due to the non-sinusoidal currents pulled from the numerous electronic devices connected to the network, there is a significant quantity of harmonics produced in energy-distribution systems. The employment of suitable active or passive filters is one of the classic methods for removing harmonic distortion in energy-distribution systems. By integrating the harmonic compensation function directly into the converter and doing away with the need for special filters, power devices based on SiC can operate at very high switching voltages and frequencies, which reduces the size, complexity and cost of the design.

Although SiC's characteristics have been known for some time, the first SiC power devices were just recently produced, beginning in the early 2000s with the use of 100-mm wafers. Most manufacturers switched over to 150-mm wafers a few years ago and, recently, although still in the research stage, large-scale manufacturing of 200-mm (8-inch) wafers.

SiC wafers' shift from 4 to 6 inches didn't go well due to the challenge of keeping the same quality and yield. The material's properties present the biggest problem for SiC manufacture. SiC takes more energy, longer and higher temperatures for crystal formation and processing due to its extreme hardness (nearly diamond-like). Additionally, because of its great transparency and high refractive index, the most common crystalline structure (4H-SiC) makes it challenging to analyze the material for surface flaws that can possibly influence epitaxial growth or final component yield.

Crystalline stacking faults, surface particles, micropipes, pits, scratches and stains are the principal flaws that might appear while making SiC substrates. On 150-mm wafers rather than 100-mm wafers, these variables, which might negatively influence the performance of SiC devices, have been seen more frequently. SiC's manufacture presents difficult hurdles in terms of cycle time, cost and dicing performance, as it is the third-hardest composite material in the world and also exceedingly delicate. Automotive and industrial markets will significantly benefit from the switch to 200-mm SiC wafers as they quicken the process of electrifying their systems and goods. As product volumes increase, it is critical for promoting economies of scale.



Power GaN Device Reliability for Widespread Power-Conversion Application Usage

By Sonu Daryanani, contributing writer for Power Electronics News

Silicon power device reliability typically follows long-established standards, such as AEC-Q100/Q101 and JESD47. Parts are typically qualified at 125°C or 150°C, with static bias applied on either the drain or gate for 1,000 hours, and a failure-in-time (FIT) rate (equal to the number of fails in 1 billion device operation hours) developed based on the number of parts tested and the acceleration profile and activation energy of the stress during these tests.

Power gallium nitride ***HEMT*** device reliability testing does not have the benefit of decades of customer experience that silicon devices have. It was noticed early in GaN power device development that the silicon device qualification process did not cover some of the main failure modes in GaN. As a result, the GaN industry worked together to form the JEDEC committee, JC70, and to develop guidelines to address GaN-specific needs. Leading GaN manufacturers like Texas Instruments (TI) have invested heavily in this effort.

In this article, we will focus on how GaN reliability is validated and highlight reliability data from TI on its GaN products.

Component level	Established framework for Si qualifications and reliablity	JESD47, AEC-Q100/Q101, JEP122
	GaN failure mechanisms, lifetime extrapolation	JEP122,JEP180
	GaN-specific test methods	JEP173: Dynamic ON-resistance test method JEP182: Continuous switching test method
Power-supply level	Switching reliablity of power management usage of GaN	JEP180: Switching reliability evaluation for GaN power devices
	Extreme operation(lightning surge,short circuit)	IEC 61000-4-5, VDE0884-11

Figure 1: Reliability testing standards and guidelines used for power GaN (Source: Texas Instruments)

TESTING STANDARDS AND GUIDELINES

As shown in Figure 1, GaN reliability testing can be categorized into component and power supply levels. Parts are qualified both under the silicon-device–developed standards, such as AEC-Q100, but additionally tested for GaN-specific failure mechanisms covered under the JEP-180, JEP-173 and JEP-182 JEDEC guidelines. Power-supply–level testing is focused on real-world situations and the impact to the GaN FET, which involves running application-specific tests for robustness from occasional events, such as power surges and short-circuits.

Let's look at some of the GaN-specific tests in more detail.

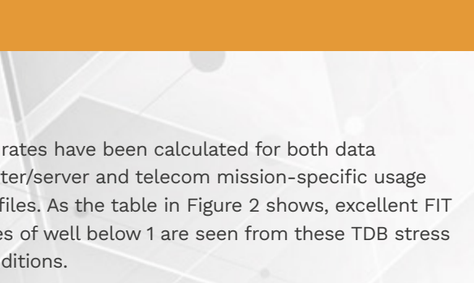
TIME-DEPENDENT BREAKDOWN

As shown in Figure 2, much like in silicon MOSFETs, time-dependent breakdown (TDB) is caused by high electric fields in several regions of the HEMT device. TI has collected data from over 1.8 million devices based on special test structures. A model has been built from this.

FIT rates have been calculated for both data center/server and telecom mission-specific usage profiles. As the table in Figure 2 shows, excellent FIT rates of well below 1 are seen from these TDB stress conditions.

CHARGE TRAPPING

Charge trapping is an occurrence wherein "traps" in the semiconductor material cause charge to stop, causing a momentary increase in resistance at the time of a FET turning on. After a small amount of time, measured in nanoseconds, the traps are full and the FET operates as expected. When the FET is turned off, these traps are released. A result of this trapping is typically an increase in the device's on-state resistance ($R_{DS(on)}$), as negatively charged traps repel the channel electrons. This increase is called dynamic $R_{DS(on)}$ degradation, as some of this trapping can be reversible and can also depend on the aging of the device. Charge trapping can occur in GaN HEMT devices in the buffer layer under the channel, in the dielectrics or at the device layer interfaces. It can occur under static conditions with a high drain bias or under dynamic switching conditions.



Datacenter and server

Load level	Time spent	Tj (°C)
10%	10%	72
20%	20%	73
50%	50%	79
100%	20%	97

10 year FIT rate calculation for LMG3422R030 part for the TDB failure mechanism (1 FIT is one failure in 10^9 operating hours)

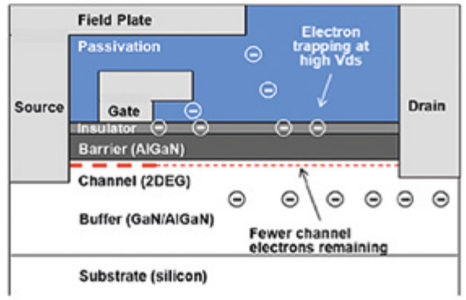
1.44 x 10^{-2} FITs for V_bus=450 V

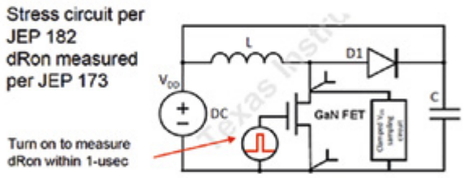
Telecom

Load level	Time spent	Tj (°C)
80%	90%	88
100%	10%	97

1.52 x 10^{-2} FITs for V_bus=430 V

Figure 2: TDB mechanism and TI data on failure rates (Source: Texas Instruments)





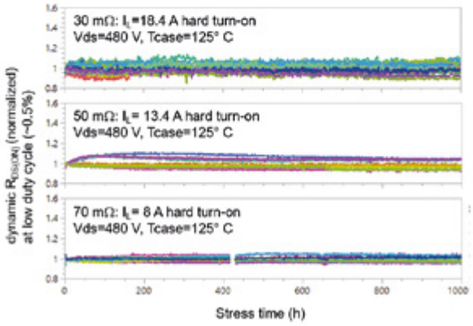


Figure 3: GaN charge trapping mechanism and dynamic $R_{DS(on)}$ measurements from TI (Source: Texas Instruments)

Low-duty–cycle, hard-switch testing can provide higher sensitivity for dynamic $R_{DS(on)}$ degradation. As shown in Figure 3, TI uses a test vehicle listed in the JEP-182 standard to provide a continuous hard-switching stress based on the maximum power condition, the maximum recommended drain voltage (V_{DS}) and the worst-case junction temperature. These conditions are per the JEP-180 guidelines.

The data over 1,000 hours of stress testing at a duty cycle of 0.5% is shown in Figure 3. This shows a stable $R_{DS(on)}$ behavior with device aging. A static off-state stress of 500-V V_{DS} at 125°C on the LMG341x GaN product similarly shows no $R_{DS(on)}$ degradation. This stable $R_{DS(on)}$ behavior in TI's GaN devices comes from many years of process flow improvements in key process steps like epi-growth as well as creating trap-free dielectrics and interfaces.

HOT CARRIER DEGRADATION

Hot carriers generated through current flow at high voltages can cause both charge trapping (resulting in dynamic $R_{DS(on)}$ increases) and create device wear-out due to defect generation. The JEP-180 guideline enables a switching lifetime to be determined

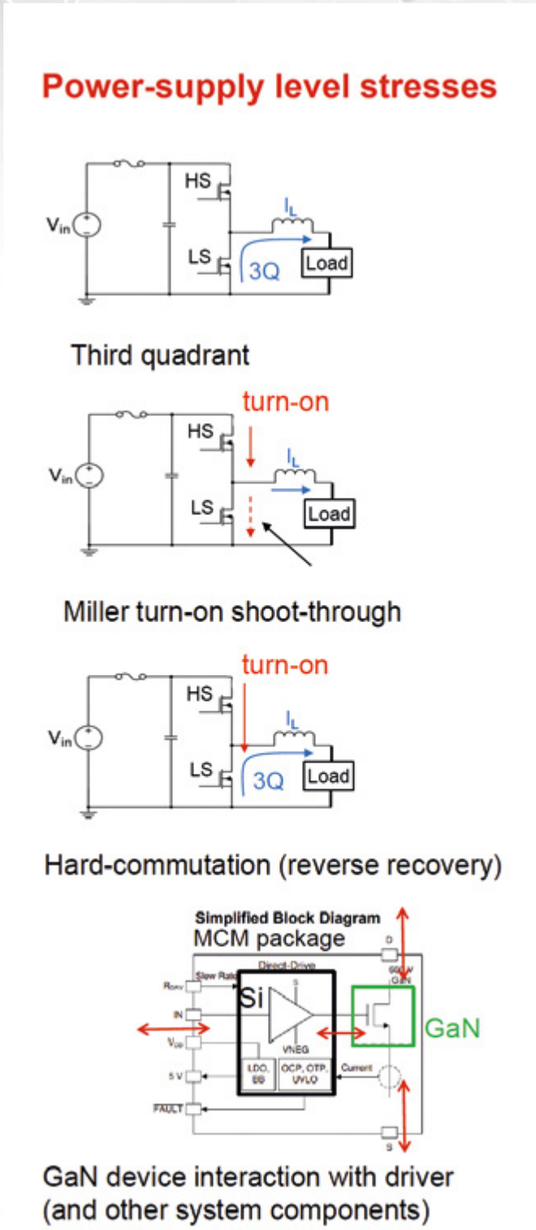


Figure 4: The DHTOL guideline of JEP-180 validates reliability for stresses of the relevant target application (Source: Texas Instruments)

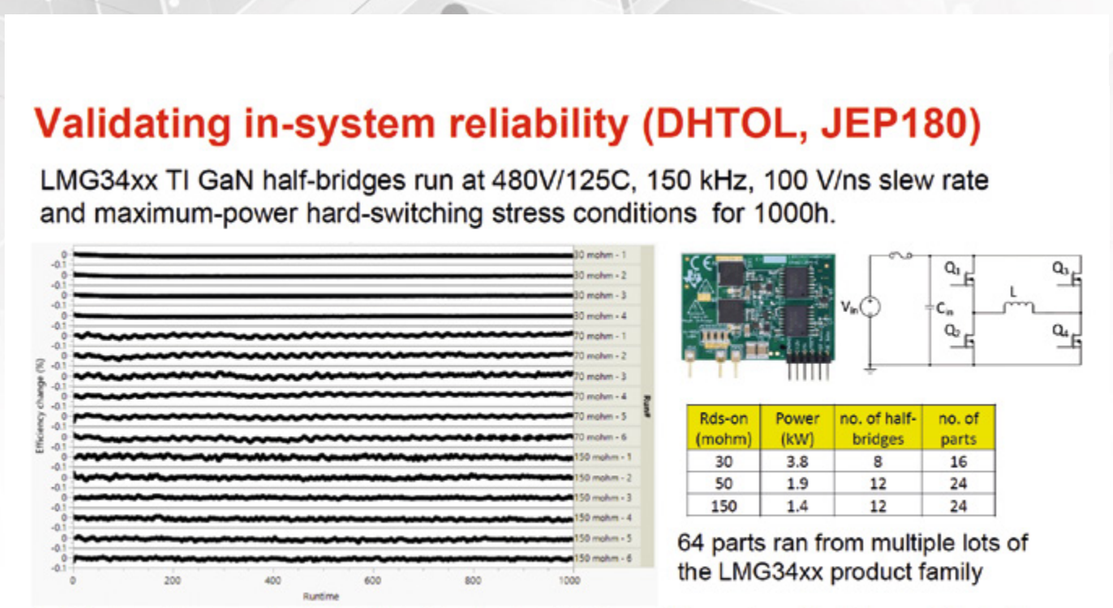


Figure 5: DHTOL test circuit and data for LMG341xx parts (Source: Texas Instruments)

from relevant stress conditions: using switching-accelerated lifetime testing (SALT). Accelerated hard-switching stress is conducted, with a 2D switching locus derived for both voltage and current acceleration. Data from these tests can then be used to build a switching stress model. This model can then be used to predict the mean time to failure (MTTF) under customer-specific conditions.

DHTOL TESTING

A key part of JEP-180 is the guideline to demonstrate that a GaN device is reliable under the stringent operating conditions in a power supply. Some of the power supply stresses are shown in Figure 4 and include conditions like third-quadrant operation and Miller capacitance–caused transient shoot-through events.

The TI dynamic high-temperature operating-lifetime (DHTOL) reliability test is based on an H-bridge circuit, as it allows power to be recycled during operation. Both hard- and soft-switching stresses are applied to the devices at high power and temperature. Conversion efficiency is monitored over a 1,000-hour stress period. Data from the LMG34xx parts, shown in Figure 4, at 480 V and 125°C show efficiency within 0.1%.

SURGE ROBUSTNESS AND SHORT-CIRCUIT PROTECTION

A voltage or current surge in a power-line–connected application can be rare, but the requirement to withstand these is essential for power supplies. The IEC 61000-4-5 specifications provide specific surge test specifications. Unlike silicon devices, GaN HEMT devices do not avalanche. Due to the limited headroom of silicon power devices between their rated and breakdown voltages, the avalanche robustness is considered a metric for surge capability.

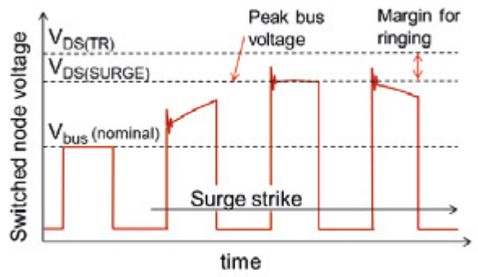


Figure 6(a): $V_{DS(SURGE)}$ and $V_{DS(TR)}$ datasheet specifications for TI's GaN devices (Source: Texas Instruments)

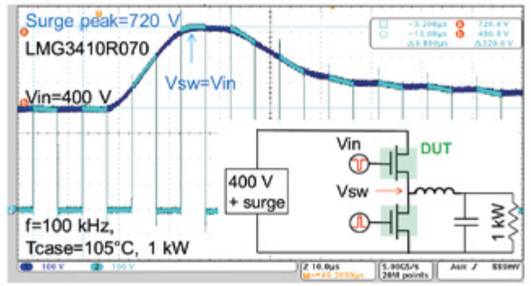


Figure 6(b): Surge waveforms for the LMG3410R70 device showing switching (light blue curve) operation during the V_{IN} (dark blue) surging to 720 V (Source: Texas Instruments)

TI has described in a ***technical paper*** the surge robustness of the LMG3410R070 part. GaN's superior transient overvoltage capability enables it to switch through surge events without avalanching. A transient surge voltage rating ($V_{DS(SURGE)}$) is specified, which is the peak bus voltage that the device can withstand during active operation. In this example, $V_{DS(SURGE)}$ is specified at 720 V, based on system considerations and customer feedback, much above the operation voltage maximum specification of 600 V.

As shown in Figure 6(a), a $V_{DS(TR)}$ ringing voltage is also specified. In this case, $V_{DS(TR)}$ is 800 V, giving an 80-V headroom over the $V_{DS(SURGE)}$ rating.
In Figure 6(b), the device surge curves are shown as it is powering a 1-kW load. In this case, 50 surge strikes were used, and there was no loss of efficiency, demonstrating surge robustness.Further, the LMG341x parts have built-in short-circuit protection. Co-packaged integration of the silicon driver and protection circuitry with the GaN HEMT allows for fast protection and turn-off within 100 ns, as shown in Figure 7.

"At TI, we take all aspects of GaN reliability seriously," said Sandeep Bahl, Distinguished Member of Technical Staff at TI. "TI has leveraged its many decades of silicon technology development, while recognizing the new opportunities that GaN brings, to think differently on how to deliver a robust and reliable power solution. TI GaN devices are reliable at both the component level and in real-world applications. They have passed both silicon qualification standards and GaN industry guidelines. In particular, TI GaN products pass JEP-180, demonstrating that they are reliable for power supply usage."

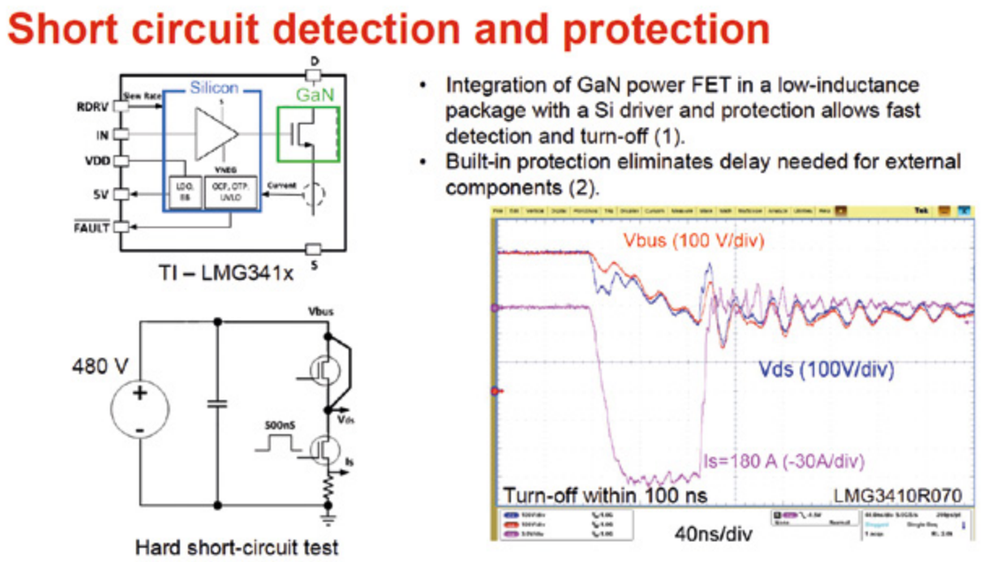


Figure 7: Short-circuit protection with the LMG341x parts showing a fast turn-off response (Source: Texas Instruments)

Supporting 48-V Conversion in Data Center Computing, Telecoms

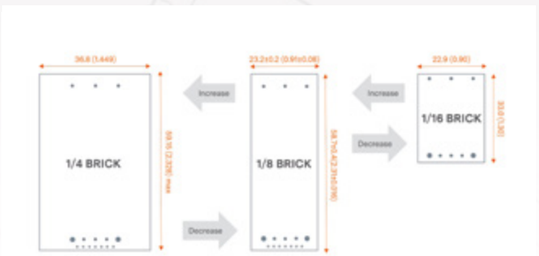
System architects are looking for improved power-conversion efficiencies that support higher rack-power ratings while driving down energy use, minimizing thermal dissipation and reducing ongoing operating costs.

By Andy Brown, director of technical marketing for DC/DC products for industrial power at Advanced Energy

The requirements for powering a modern server are largely defined by the computing capability of that server. As the servers become more capable, their power requirements also increase. Efficiency is critical, as it not only reduces operating expenses but allows for smaller power solutions with enhanced power density.

With high capital costs for equipment and space and rising energy costs, incremental efficiency gains make a significant impact for server farms, where thousands of servers are deployed simultaneously. Increased efficiency also reduces the load for air conditioning for cooling the building, saving capital and operating expenses. Ultimately, the goal for any power solution is to reduce the total cost of ownership of the entire system and increase the functionality and performance of the server.

Traditionally, data center power solutions convert incoming grid supply voltage to lower-voltage three-phase mains voltage that is converted locally in rack-mounted servers to 12 VDC (the preferred voltage for many components, including motherboards and peripherals like hard drives). However, with some 19-inch rack cabinets now requiring 30 kW, a 12-V distribution voltage presents challenges for distributing and converting power from AC/DC converters mounted in a sub-rack, which is remote from the server. Current, for example, can reach 2,500 A, which is far from



Fractional bricks are a range of power modules with de facto industry-standard sizes and footprints.

practical due to the impact of power loss and voltage drops related to connections within and from the cabinet.

Responding to this, in 2016, the Open Compute Project (OCP) began to drive toward 48 V as a standard for servers and distribution within data centers. The choice of 48 V was to reduce current by a factor of 4 (delivering a sixteen-fold reduction in I^2R losses). Additionally, 48 V can be viewed as safer with extra-low voltage (ELV) or separated extra-low voltage (SELV) depending on grounding, meaning that isolation can be removed from the power path, delivering a consequential efficiency increase.

The change to 48 V is reflected in the Open Rack Base Specification, now at version 3 (ORv3). Alongside stipulations for the mechanical design of racks, this document defines voltage specifications for the input voltage (either 51 VDC or 54 VDC) as well as current ratings for key components and the need for voltage sensing. It also specifies that the bus voltage remain lower than the 60-VDC limit of ELV.

At the same time, many areas of servers are heavily committed to 12 V—not least motherboards, PCIe slots, memory and hard drives. Designs for 12 V are well understood and supply chains are fully established. As a result, the need for a 12-V rail within mainstream servers will continue for the foreseeable future.

DELIVERING EFFICIENT 48-V TO 12-V CONVERSION

With many of the modern processors requiring up to 700–800 W of power, many power solutions for servers tend to be in the 800-W to 1-kW region, with 900 W being highly popular. Almost exclusively, 48-V to 12-V conversion uses the so-called “brick”-derived form factor. The term “brick” was coined over 20 years ago to describe a PCB-mount package with an approximately 4.6 × 2.4-inch footprint.

As technology evolved, smaller versions of the brick package evolved, known as fractional bricks. These ranged from a half-brick down to the 1/16 brick, although the size ratios are not exact. As these footprints have become a de facto industry standard, server design engineers can easily implement these standardized brick packages during the design process and users are able to multi-source with relative ease, giving them assurance of supply.

However, with ability to radiate heat being linked to physical size, there is a finite amount of energy that can be removed from each size of brick. This is now the limiting factor in the amount of power that each fractional brick form factor can deliver for a given efficiency level. For example, we could assume that a quarter-brick could dissipate 25 W, which, for example, corresponds to a 500-W device at 95% efficiency. Increasing the power output to 900 W with the same 25-W loss would imply an efficiency of 97.3%.

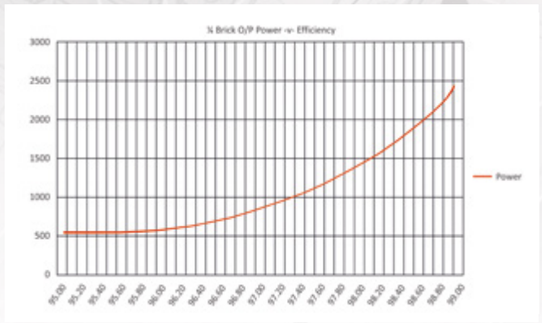
Today, we are at an inflection point in terms of the relation between efficiency and power, with increases in efficiency shifting from a relatively proportional to a more exponential relationship with power. Thus, as efficiency rises toward 100%, each incremental improvement leads to a much more significant improvement in power capability.

Many 48-V bricks include isolation as a result of their use in telecom systems. In these bricks, the 48-V input rail has negative polarity, so galvanic isolation is required to invert the output for positive polarity. For 48 VDC, the server supply voltage is positive polarity; therefore, no inversion and no isolation is needed, as noted in the OCP proposals. The removal of the requirement for isolation can yield an (approximate) 0.3% improvement in overall efficiency, thereby increasing the power capability of the brick.

Similarly, removing the output voltage regulation from a brick converter can yield an (approximate) 0.5% increase in efficiency. Given that the 48-VDC input voltage is comparatively tightly regulated, one might assume this would be another realizable benefit.

For the majority of components, this would be true, but memory (DIMMs) and PCIe cards require a highly regulated 12-VDC supply, so being that a single brick is used for the 48-V:12-V conversion function, a regulated output remains by far the most sensible and popular choice.

As servers become more sophisticated, so do the power solutions they rely upon. Many supplies now



The effect of incremental efficiency improvements unlocks more power as overall efficiency increases.

incorporate the Power Management Bus (PMBus). This was originally developed by several companies, including Artesyn Embedded Technologies (now part of Advanced Energy), as a standard means of communicating with a power device over a digital communication bus, allowing a system processor to configure, control and monitor voltages, currents and temperatures.

This has significant benefits during the design phase and can be valuable during operation to confirm that the system is working as expected, as well as give early warning of any impending faults by monitoring the function of power conversion from within the power module.

Current sharing is an important feature that allows the outputs of several bricks to be combined to deliver higher power. Passive (aka "droop") sharing is the simplest approach, as it does not require bricks to be interconnected with a current-share bus signal and it is relatively immune to startup inrushes and other transients. However, it has limitations. The most significant is the need for a softer output voltage load regulation characteristic that results in greater than 200 mV of "droop" required to enable accurate load sharing between units. There is also the need for a fold-back current-limit characteristic, as the standard overcurrent protection method of hiccup mode is not appropriate in current-sharing applications. As a result, active sharing to control and force units to share accurately is the preferred choice for regulated devices.

TECHNOLOGY EXAMPLE

One example of a modern brick converter intended for use in server applications is Advanced Energy's Artesyn NDQ900. This quarter-brick non-isolated DC/DC converter unit provides a single regulated low-noise output of 12.25 V from an input range of 40 to 60 VDC at continuous power levels up to 900 W (73.7 A).

The highly efficient design achieves a peak efficiency of 96.7%, and with the built-in baseplate, heat can be dissipated by contact cooling or via a directly attached heatsink. The fixed switching frequency benefits EMI performance and permits simple filtering where necessary.

The unit includes the advanced PMBus functionality for configuration, control and monitoring and multiple units may be used in parallel with the in-built active current sharing. A range of valuable protections are provided, including input undervoltage/overvoltage, output overvoltage/overcurrent, and overtemperature.

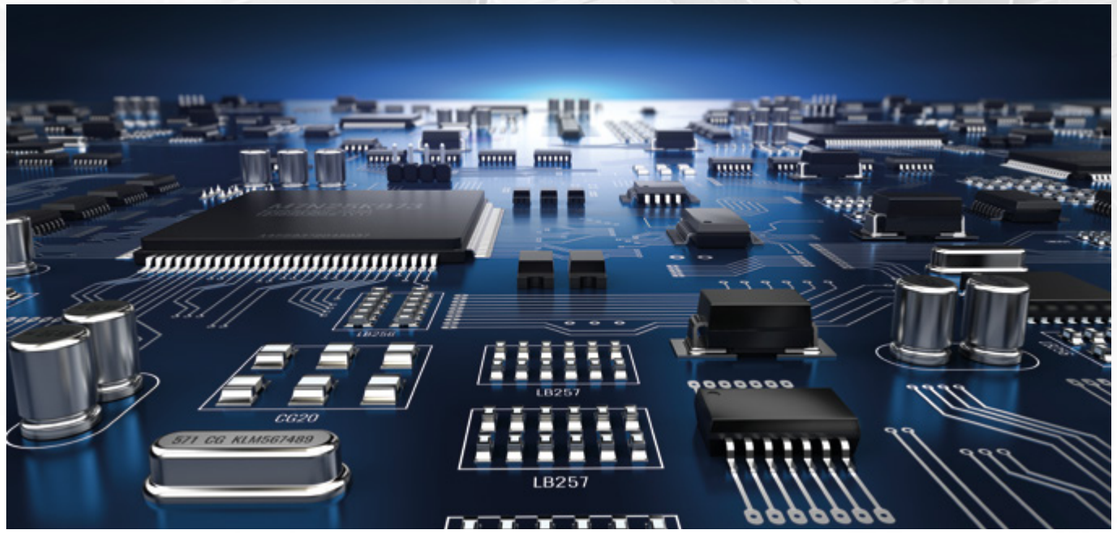
LOOKING AHEAD

The worldwide server market continues to show strong growth with a 17% CAGR from 2022 to 2027, according to Dell'Oro Group's Data Center IT Capex 5-Year Forecast Report (January 2023). The largest users have in excess of 3 million installed servers, and some companies are projected to reach over 10 million installed servers by 2027. Indeed, servers represent a very significant percentage of energy use globally, and their share of DC capex is predicted to grow to 57% by 2027.

This sheer scale of global data center operations underlines the huge benefits of even small gains in efficiency, with every single watt of power saved in power-conversion losses representing not only 1 W less to be supplied but also 1 W less that requires cooling by data center cooling solutions.

Power technology must continue to advance to make servers fit for the future in terms of efficiency, size and overall energy usage. The choice of converter technology is critical to transform the emerging 48-V intermediate bus to the conventional 12 V that continues to be required. Additional innovations to those discussed in this article will address the increasingly demanding requirements in new and emerging servers.

Advanced Energy's Artesyn NDQ900 series 900-W quarter-brick non-isolated DC/DC converter



Building Semiconductor Capacity for a Hotter, Drier World

By Katherine Bonamo, contributing writer for Power Electronics News

As recently as four years ago, few economists would have predicted some of the major news items of the past few months. Few would have expected to see Ford blame a quarterly-sales shortfall of 100,000 vehicles on its inability to buy the right microchips. And still fewer might have expected a spike in semiconductor fab construction within the borders of the United States. But a global pandemic was enough to make just about everyone guess wrong.

With the world's reliance on microchips in sharp relief—and with a boost from the CHIPS and Science Act of 2022—semiconductor fab construction on U.S. soil is booming. The Semiconductor Industry Association reports that since 2020, over $200 billion from more than 35 companies has been pledged toward chip-related manufacturing projects in the United States.

Meanwhile, a crisis longer in the making looms just as large. According to the National Oceanic and Atmospheric Association, the last eight years have been the hottest on record, and the impact on the world's weather has been hard to ignore. High temperatures trigger heavy downpours in some areas while exacerbating drought in others.

The potential for these issues to collide is clear. The semiconductor industry is water-intensive: A single fab's needs can run into the tens of millions of gallons per day, outpacing the household requirements of a small city. In drought-stricken Arizona, Intel and Taiwan Semiconductor Manufacturing Company (TSMC) are both investing billions in new facilities—while farmers already face water rationing. Nor can chipmakers afford to ignore their overall carbon footprint—not when tech giants Apple, Google and Microsoft have all committed to reaching net-zero emissions throughout the entire supply chain.

From this point of view, the boom in U.S. fab construction represents an opportunity as well as a challenge. To operate in a world where resources must be conserved to the utmost, both new approaches and long experience will be required. Luckily, both can be found through design partnerships with sophisticated suppliers like GF Piping Systems.

THE PRICE OF ENTRY

The baseline technical standards required for the infrastructure in a semiconductor fab are high to begin with. The slightest contamination from dust can jeopardize product quality, so fabs typically operate under the cleanest of "cleanroom" conditions (ISO Class 1). High purity standards must also be applied to the lifeblood of a semiconductor fab: its water supply. As the millions of transistors, resistors and capacitors in a chip's integrated circuit are built up on the substrate of a silicon wafer, layer by layer, rinsing is required at many points. This part of the process is essential, as even trace amounts of impurities remaining could change the wafer's electrical properties.

To succeed in removing contaminants without adding new ones, fabs must use ultrapure water (UPW) for rinsing. UPW has been purified of all other molecules to the point that it very nearly approaches 100% H_2O. Approximately 1,400–1,600 gallons of municipal water are needed to create 1,000 gallons of UPW. The resulting product's chemical properties are so different from tap water (including its resistivity of 18.2 MΩ) that it is not safe for humans to consume.

Given the effort and expense involved in buying or creating UPW (which requires an elaborate three-stage process to make), semiconductor fabs must also ensure that their fluid transport systems meet equally high standards to avoid reintroducing unwanted substances. A single fab site may include up to 40 km of piping for the transport of UPW, and the conditions under which that piping was made matter just as much as conditions in the fab itself.

As noted by Ted Sinclair, global sales manager for microelectronics at GF Piping Systems, any source of contamination is unacceptable "in a process where the distance between each transistor is measured in nanometers. Our components make sure that nothing impure makes its way into the manufacturing process on a molecular basis. The reality is, it's both the high-purity resin we use and the purity of the pipe-extrusion environment, the cleanroom in which we extrude the pipe, that deliver the high-purity results our customers demand."

The Sygef Plus fluoropolymer piping system is manufactured by GF from carefully screened materials under ISO Class 5 cleanroom conditions. Rigorous testing, special packaging measures and highly reliable jointing technologies for assembly also serve to ensure the high purity of final installations.

EVERY DROP IS PRECIOUS

With dried-up lakes and rivers making worldwide news last summer, it has never been more obvious that responsible use of water is essential. To continue and even increase water-hungry semiconductor production, it will be equally essential to adopt a recycling mindset from when shovels hit the ground.

Dominik Roth, global business development manager of sustainability at GF Piping Systems, pointed out that "circulating water to reduce consumption is paramount." And for reasons of both economics and community relations, semiconductor manufacturers are taking note. Reuse of wastewater for cooling purposes is a common first step, but interest in the more complex process of reclaiming waste streams as feedwater for UPW systems is increasing.

At one time, it was common for semiconductor manufacturers to recycle only about 40% of their wastewater, forcing them to find less sustainable treatment and disposal strategies for large volumes of water contaminated with toxic solvents or heavy metals. But by the mid-2010s, TSMC was able to report process-water–recycling rates of over 85%. Similarly, for 2021, Intel reported using 16 billion gallons of fresh, reclaimed or desalinated water for manufacturing—but also reported returning 13 billion gallons to surrounding communities or the environment.

Planning for on-site water recycling at the construction stage can thus build sustainability into a plant's operations right from the beginning, and here again, an experienced design partner can help. With expertise in both process automation and fluid transport, "GF has been supporting the semiconductor industry's efforts to build the most sustainably managed fabrication factories for more than 30 years," Sinclair said. "Thoughtful collaboration and system modeling from early in the project, with a vertically integrated single partner from system design through product manufacturing—that can really elevate the final result."

MAKE IT WHERE YOU NEED IT

Perhaps unsurprisingly, the overall energy demands of semiconductor manufacturing are considerable. A typical fab might use as much power in a year as 50,000 homes. A "megafab" might draw power more on the scale of an auto plant or oil refinery. To find ways to limit emissions, creative thinking may be required, and examining all aspects of the supply chain is a must.

Typically, about 20% of the greenhouse gas emissions associated with a semiconductor fab belong to the "upstream" category of "Scope 3" emissions, as defined by the widely used Greenhouse Gas Protocol. Factors like energy use for production or transportation on the part of a supplier are part of the purchaser's responsibility, even though they have no direct control over those activities. The large-scale investment required by a new fab therefore also calls for close review of supplier sustainability practices in addition to their technical competence.

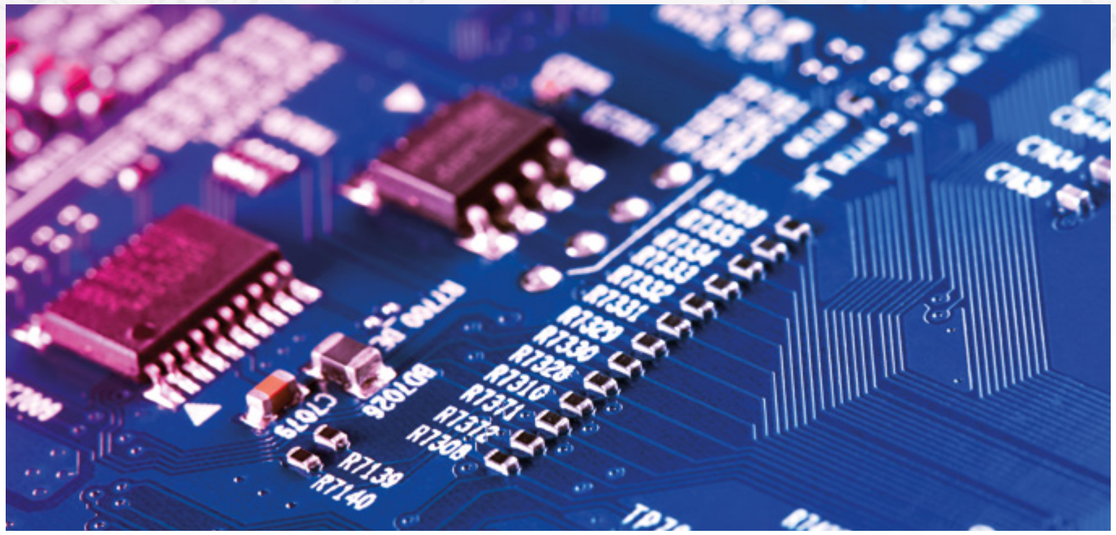
In this context, products that do not need to be transported long distances to the construction site have great appeal. In addition to other sustainability benefits, such as lighter plastic materials and the company's ongoing progress on fronts like recycling and renewable electricity, GF Piping Systems' worldwide network of prefabrication has thus become highly popular with customers. "Four out of four of the customers I spoke with today inquired about this capability, which significantly decreases overall construction duration," Sinclair said.

Experienced partners like GF Piping Systems can make semiconductor fab construction more sustainable, with options including localized prefabrication. (Source: GF Piping Systems)

To facilitate the construction process for customers, GF has invested in off-site fabrication shops close to major construction sites and is continuing to grow the network. With subassembly work conducted at the prefabrication site, GF can deliver "laterals," or partial assemblies that can be transported a shorter distance to the factory and quickly installed on-site. Existing GF prefabrication sites in the United States include Shawnee, Oklahoma; Irvine, California; and Dallas.

BUILD FOR THE FUTURE

The major crises in human history differ in the details, but they all have one thing in common: They call for a reappraisal of the way things have always been done. Semiconductors may be here to stay, but when, where and how they are made will continue to evolve. Every element in the process, right down to the pipes moving water though the factory, will come under increased scrutiny in years to come. But as a generational investment in capacity takes place across the U.S., another rare chance presents itself as well—the chance to build a more sustainable future, right from the ground up.



Cu-Clip Package Technology Empowers WBG Devices

By Maurizio Di Paolo Emilio, editor-in-chief of Power Electronics News

Strengthened by the innovations introduced with copper (Cu)-clip package (CCPAK) technology, Nexperia brings its long-time experience producing high-quality and robust SMD packaging to its gallium nitride FET portfolio. Based on proven technology, CCPAK provides industry-leading performance in a wire-bond–free package optimized for thermal and electrical performance, simplifying the design of cascode configuration and eliminating the need for complicated drivers and controls.

Nexperia introduced LFPAK technology in 2002. This was a remarkable and radical departure from the designs of the day because of the characteristic continuous clip and gull-wing terminal pins. Very low electrical and thermal resistance at the PCB level, along with a new low level of $R_{DS(on)}$, has been made possible thanks to this technology.

Surprisingly, it required some persuading to convince the industry that a device just half as big as its predecessor (DPAK) could have the same thermal performance but better electrical performance and that the novel Cu clip was more reliable than bond wires. Over 400 devices spanning seven design variants, or about 90% of Nexperia's product line, are LFPAK-based and contribute to a design's overall efficiency.

IT ALL STARTED WITH LFPAK

In automotive and industrial applications, the need for high power has increased in modern electronics. Kilowatt power output is a typical requirement for applications like motor drives, inverters or on-board chargers. This means the need to handle greater power is being transferred to the components, especially MOSFETs, due to existing space constraints in modules.

LFPAK technology was designed to address the challenging requirements coming from power electronics applications. Compared with conventional wire-bond devices, LFPAK offers several advantages, including compact size, higher power density and reduced parasitic inductance. Based on Cu-clip bond technology, these packages have played an essential role in allowing silicon-based MOSFETs to achieve very high-current capability.

Compared with D2PAK technology, based on wire bond, LFPAK offers the following benefits:

- Prevents localized current crowding
- Allows for a more uniform current spread
- Acts as a heatsink to the die

The internal structure of an LFPAK MOSFET is shown in Figure 1. Cu clips can withstand very high temperatures, as the melting temperature of copper is about 900°C. The silicon die, due to the doping process, can operate up to 250°C without compromising the switching performance. The plastic mold compound, whose composition is carefully selected to withstand high-temperature specification, can potentially harden and becomes brittle at about 190°C and above. As a result, the internal components of the MOSFET are either naturally capable of withstanding temperatures >175°C or specifically selected to do so.

The maximum junction temperature of MOSFETs is limited to 175°C due to the reliability standards that MOSFETs must adhere to. By industry standards, Nexperia uses a temperature limit of 175°C for MOSFET qualification and life testing.

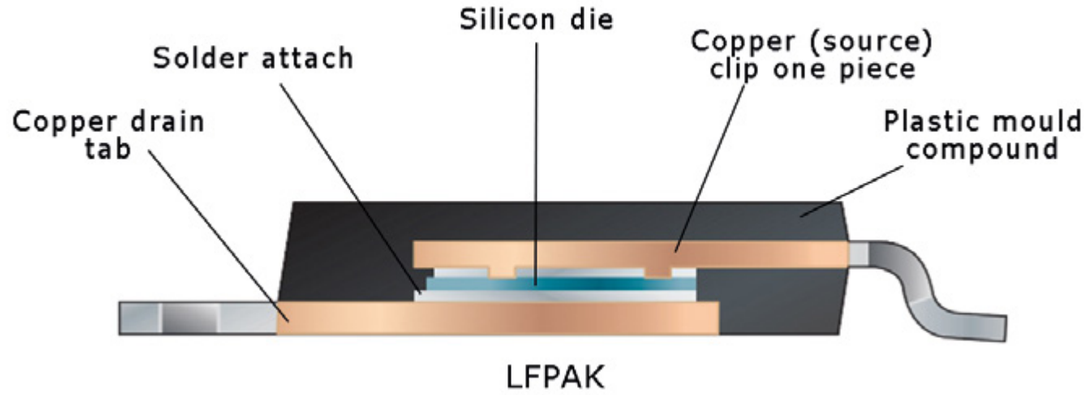


Figure 1: LFPAK internal structure (Source: Nexperia)

The computing industry requires exceptionally high current to power the newest generation of processors and microcontrollers, which is why Nexperia created LFPAK technology. The peak current started approaching 200 A and beyond as each new silicon technology node brought on-chip exponentially more transistors while reducing the supply voltage. Because the standard SO-8 transistor package couldn't handle it all, power supply designs had to become more complex, using larger packages like DPAK and even D2PAK.

To replace DPAK or D2PAK, LFPAK56 was developed to provide greater power from the widespread SO-8 package footprint. Despite having less than half the footprint size (LFPAK's 30 mm², compared with DPAK's 70 mm²), the initial generation of 25-V MOSFETs in LFPAK56 (which owes its name to its size of 5 × 6 mm) exhibited $R_{DS(on)}$ and maximum drain current equivalent to identical devices in DPAK. Because of its enormous cross-sectional area, the Cu-clip attachment, which substitutes conventional bond-wire connections between the die and leadframe, significantly improves electrical and thermal performance.

How LFPAK56, at less than half the size of DPAK, could achieve equal thermal performance baffled the industry at first. Although the physics of soldering the clip directly to the source connection on the device eliminated the high-current–density regions that often exist where bond wires are joined, others questioned the clip attachment's reliability. Consequently, a Cu clip shields the transistor by preventing the development of thermal "hotspots" at specific sites.

Testing for reliability and thermal performance demonstrated that LFPAK could deliver on its promises. Moreover, LFPAK56 passed the demanding 2× AEC-Q101 automotive qualification, exceeding all standards by a wide margin.

The Cu clip also lowers package inductance, which is 3× lower than traditional wire-bonded packages, allowing for higher switching efficiency and less electromagnetic interference (EMI). In today's power supply designs, which aim for higher frequencies to provide greater power density and faster dynamic response, boosting switching efficiency is becoming increasingly crucial.

CCPAK ADDS SUPPORT FOR WBG SEMICONDUCTORS

The natural evolution of LFPAK technology is CCPAK, developed to boost the power handling, electrical efficiency and reliability capabilities offered by the incoming generation of wide-bandgap (WBG) devices.

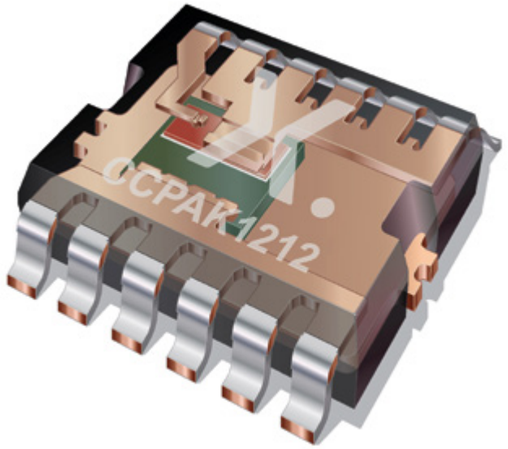


Figure 2: A CCPAK1212 GaN FET power device (Source: Nexperia)

The Cu-clip technology from Nexperia has revolutionized the power packaging industry and has set the standard for performance and efficiency ever since. With the introduction of Cu clip in 2002, over 90% of Nexperia's product line now utilizes the LFPAK loss-free package. This technology is prominent in the new CCPAK1212, shown in Figure 2, which houses Nexperia's most recent GaN FETs.

The main features of this latest innovative package can be summarized as follows:

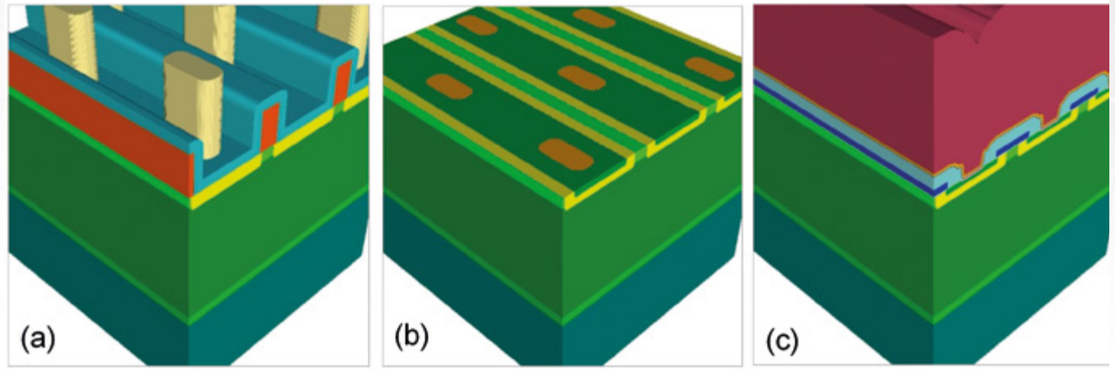
- Small form factor (12 × 12 mm) and low package height (2.5 mm) compared with traditional through-hole packaging like TO-247
- Wire-bond–free for low inductances and ultra-low package resistance; Cu clip offers 3× lower inductances than industry-standard packages for lower switching losses and EMI
- Flexible gull-wing leads that offer higher board-level reliability and easy optical inspection that gives compatibility with SMD soldering and automatic optical inspection
- Excellent thermal performance with thermal resistance of typically less than 0.5 K/W, providing optimal cooling and operating with a maximum temperature of 175°C
- Two cooling options available: bottom-side cooling (CCPAK1212) and top-side cooling (CCPAK1212i)

CCPAK1212 is an ideal package for Nexperia's GaN-based power transistors. GaN and Cu clip are a great match, as WBG technology can provide outstanding efficiency in fast-switching circuits, meeting even the most demanding requirements coming from the automotive industry.

Nexperia shipped over 1.7 billion pieces in 2021 and another 1.9 billion pieces in 2022 (LFPAK devices, including MOSFETs and bipolar power transistors in the LFPAK56 and its later versions, which ranged in size from the smaller 3 × 3-mm LFPAK33 to the larger 8 × 8-mm LFPAK88). With the addition of the new CCPAK1212 to the Cu-clip product portfolio, Nexperia believes this technology will continue to play a significant role in cutting-edge power semiconductors for many years, whether employing GaN or SiC or MOSFET devices.

Reference

[1]Yandoc, D. (Dec. 16, 2022). *"How Copper Clip Makes Perfect Packages for the Future of Power."* Blog post.



A Deep Dive into ST's Third-Gen Automotive-Grade SiC MOSFETs

By Deyan Chen and Stephen Russell, subject matter experts at TechInsights

Toward the end of 2022, STMicroelectronics introduced its third generation of "STpower" silicon carbide MOSFETs, advanced power devices for electric-vehicle and fast-charging EV infrastructure applications in which power density, energy efficiency and reliability are critical. Devices with nominal voltage ratings from 650 V up to 1,200 V are currently available and will garner significant attention in the market due to ST's previous design wins with automotive manufacturers like Tesla.

SCT040H65G3AG, one of the first available products in STMicroelectronics' third generation of STpower SiC MOSFETs, is a 650-V (drain-source), 30-A, 40-mΩ on-resistance enhancement-mode N-channel SiC power MOSFET. The SCT040H65G3AG die, a detailed process flow and comparisons with Generation 2 and other vendors' SiC MOSFETs will be discussed.

SCT040H65G3AG 650-V SiC MOSFET

TechInsights has completed multiple process analysis reports for SCT040H65G3AG die in the Power Semiconductor subscription, including a floorplan report (***PFR-2207-803***) that offers identification of the key functional blocks in the analyzed die, process identification and manufacturing cost. Also completed is a Power Essentials (PEF) report (***PEF-2207-802***) presenting in-depth process, structural, material analyses and examinations of the dopant distribution of all active layers.

Like the second-generation ***SCTH90N65G2V-7*** SiC MOSFETs, the SCT040H65G3AG die features a vertical planar-gate SiC MOSFET encapsulated in a seven-lead H2PAK package with 10.23 × 10.13 × 4.45-mm dimensions and an additional "driver source" pin, as shown in Figure 1. The SCT040H65G3AG package comprises a

single SiC die and seven pins for the gate (G, one pin), driver source (DS, one pin) and power source (PS, five pins), the exposed lead frame is present at the back of the package and connected to the drain terminal of the SiC MOSFET.

The SCT040H65G3AG die features a vertical planar-gate design with a pitch of 4.8 µm, planar polysilicon gate and single thick pre-metal dielectric deposited on the polysilicon to isolate the gate from the source/body metal.

To further investigate the workings of the SiC MOSFET, scanning capacitance microscopy (SCM) was undertaken to describe the dopant distribution in all active regions.

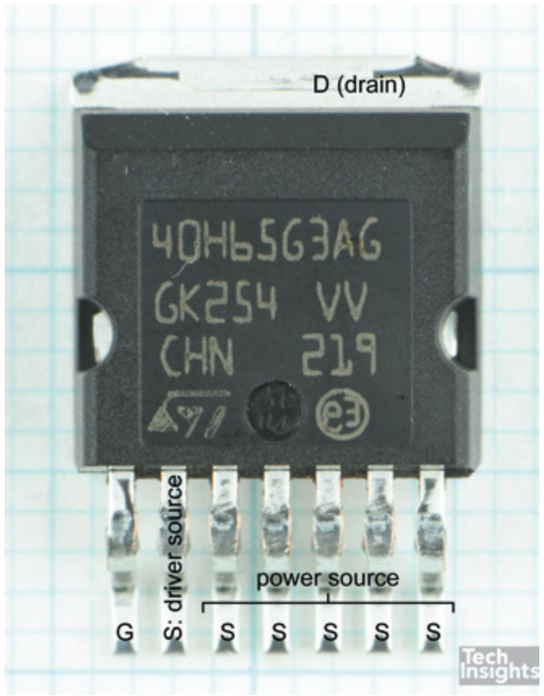


Figure 1: STMicroelectronics' SCT040H65G3AG in a seven-lead H2PAK package

PROCESS FLOW ANALYSIS OF SCT040H65G3AG

In addition to the empirical analysis of reverse-engineering results in PFR and PEF channels, the SiC process flow channel is mainly built based on the interpretations of the discovery of PEF, and the manufacturing steps of the selected SiC power devices are reconstructed in detail in this channel.

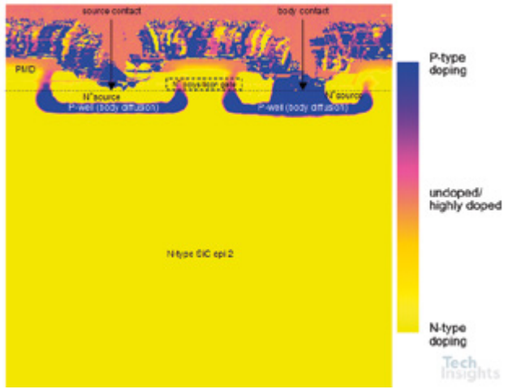


Figure 2: SCT040H65G3AG active SiC MOSFET cell SCM image

The Process Flow Full (***PFF***) analysis further expands on the PFA results and produces an interpreted mask set, which is then used as an input to carry out verification and fine-tuning of the manufacturing steps outlined in the PFA. Thanks to ***Synopsys Sentaurus Process Explorer*** software, the PFF report is executed to help understand the whole process flow easily through visual 3D emulation.

MARKET-LEADING 650-V SiC MOSFETS: FEATURES AND PERFORMANCE COMPARISON

In our original 650-V SiC MOSFET comparison blog from last year, we compared device on-state performance—namely, the on-resistance ($R_{DS(on)}$) and specific on-resistance ($R_{DS(on)} \times A$), which are treated as standard metrics in power MOSFET technology.

Both STMicroelectronics' second and third generation stick to a planar polysilicon gate and stripe cell layout. Compared with STMicroelectronics' second generation, the $R_{DS(on)} \times A$ in the active array of the third-generation product has been reduced ~40%, from 2.75 mΩ·cm² to 1.64 mΩ·cm². This is achieved by a ~20% lower gate array pitch and dopant distribution optimization of drift region, making this device's conduction performance similar to other leading SiC planar MOSFETs, such as Wolfspeed's C3M0015065D with 1.99 mΩ·cm², albeit ST's device is driven @ V_{GS} = 18 V. It surpasses onsemi's NTH4L015N065SC1, which has 2.51 mΩ·cm² @ V_{GS} = 18 V.

Both Wolfspeed and onsemi employ a hexagonal cell layout that gives a densely packed and scaled cell design with significant advantages when it comes to on-state performance. Despite the cell pitch of Wolfspeed's C3M0015065D device being larger, it still maintains a low value of 1.99-mΩ·cm² on-resistance, even at a gate bias of 15 V. The reasons for this were

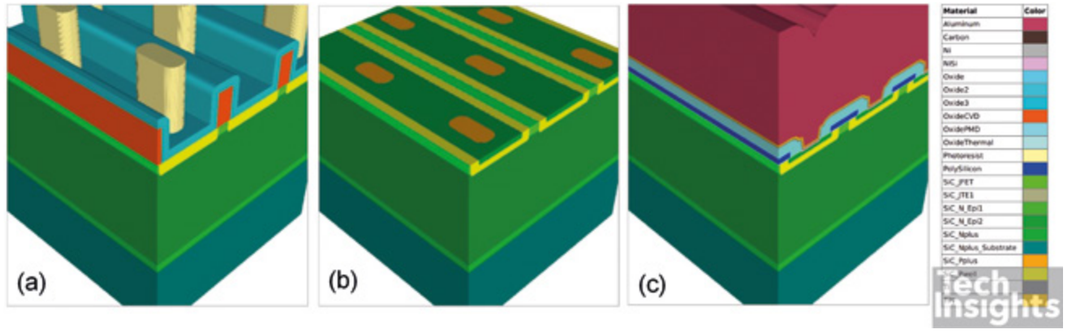


Figure 3: Selected 3D emulation results at various stages of the STMicroelectronics SCT040H65G3AG flow — (a) right after P⁺ blocking lithography; (b) at the completion of P⁺ implant module; (c) just after top metal deposition

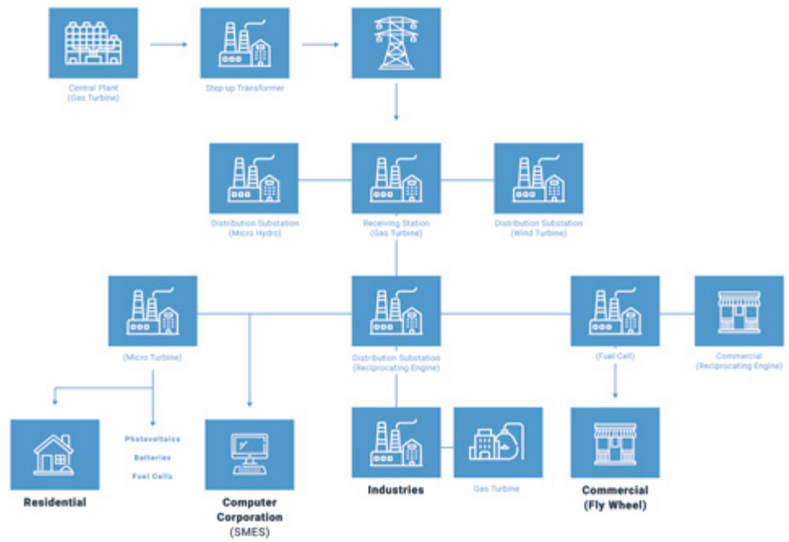
discussed in our ***blog*** "Reviewing Approaches to SiC MOSFET Cell Design."

In vertical power SiC MOSFETs, trench-gate designs can bring an on-state performance advantage, although significant shielding is often needed to protect the trench regions, as also discussed previously. Given the automotive applications of STMicroelectronics' device, it makes sense that ST has stuck with the somewhat-conservative planar gate rather than trench to avoid any tricky issues with device robustness.

CONCLUSION

The 650-V class of SiC MOSFETs is one of the hottest topics in the power semiconductor market, with potential applications spanning many high-growth markets, not least automotive. STMicroelectronics' automotive-grade third-generation 650-V SCT040H65G3AG SiC MOSFET was selected last year by TechInsights as a candidate to offer a complete analysis, including SiC Power Floorplan, PEF, Process Flow Analysis and PFF reports. For details of our complete Power Semiconductor subscription offerings, please see the ***Power Semiconductor Product Vertical Overview***.

Four years after STMicroelectronics delivered its second-generation product, without a big change in the device layout (still employing the scheme of planar polysilicon gate and stripe cell layout), it successfully elevated its third-generation 650-V product performance to compete with leading competitors by reducing the cell pitch and possibly optimizing dopant distribution of the drift region. Coupling this with STMicroelectronics' previous success with automotive-grade SiC MOSFETs makes this part a formidable entrant to the market.



3.3-kV SiC MOSFETs Enable Grid-Connected Energy Storage

By Ranbir Singh, executive vice president, and Siddarth Sundaresan, senior vice president of SiC technology and operations, both at Navitas Semiconductor

The grid supplies energy from generators and delivers it to customers via transmission and distribution (T&D) networks. In the U.S., use of electricity storage to support and optimize T&D has been limited due to high storage costs and limited design and operation experience. Recent improvements in storage and power technologies, however, coupled with changes in the marketplace, herald an era of expanding opportunity for electricity storage.

Figure 1 illustrates the future vision for electricity production and T&D infrastructure, identifying grid-connected storage as critical for more reliable, more cost-effective models. Energy storage improves T&D performance by compensating for electrical anomalies and disturbances like variations in voltage (e.g., short-term spikes or dips, longer-term surges or sags), variations in the primary frequency at which power is delivered, low power factor (voltage and current excessively out of phase with each other), harmonics, (the presence of currents or voltages at frequencies other than the primary) and interruptions in service.

Utility-attached storage reduces costs by allowing purchase of inexpensive electricity during periods of low demand and supply of that energy when the price would otherwise be higher. Storage may also be used in lieu of adding generation capacity. In many areas, transmission capacity is not keeping pace with peak demand, meaning transmission systems are becoming congested—driving increased transmission access charges and use of congestion charges or “locational marginal pricing.”

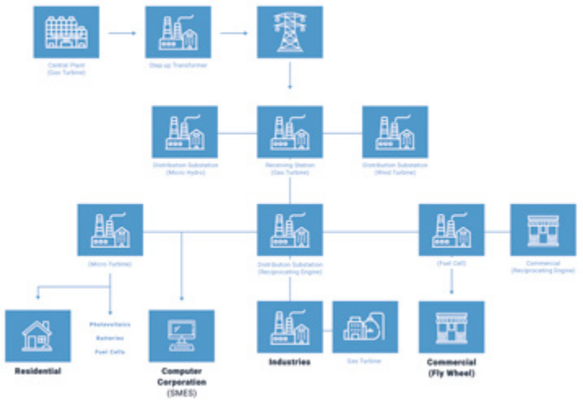


Figure 1: Grid-connected energy-storage elements are critical to future power T&D.

Storage is also increasingly used to balance out intermittent power supplies from renewable-energy resources like wind and solar.

SiC DRIVES STORAGE INNOVATION

Use of all-SiC inverters will revolutionize electricity delivery, renewable-energy integration and energy storage. It is well recognized that silicon-based semiconductors have inherent limitations that reduce their suitability for utility-scale applications. With SiC, however, power electronics applications including static transfer switches, dynamic voltage restorers, static var compensators, high-voltage direct-current transmission and flexible alternate-current–transmission systems all become economically feasible. With SiC, medium-voltage (MV) inverter manufacturers can realize efficiencies of >97.8% at 100 kW to 1 MW, allowing more compact inverters to be deployed at large scale across residential and industrial implementations.

INTEGRATING BESS WITH MV GRID

A battery energy storage system (BESS) is integrated to an MV grid (2.3 kV, 4.16 kV or 13.8 kV) using an isolated topology like a dual active bridge (DAB) followed by an active front-end converter. A three-level (neutral-point–clamped) topology reduces both the filter requirements compared with a two-level topology and the voltage stress across the SiC MOSFETs. Depending on grid voltage, a series connection of the SiC 3.3-kV MOSFET diode devices is possible, as shown in Figure 2. Additional topologies can also be considered for analysis. The low-voltage (LV) side is made through 1,200-V SiC devices. In the DAB, the MV transformer (LV to MV conversion) can be operated between 10 and 20 kHz. A single-phase or a three-phase system can be used depending on the power requirements.

The MV SiC MOSFETs' fast-switching transients can result in a dV/dt as high as 100 kV/µs, imposing a

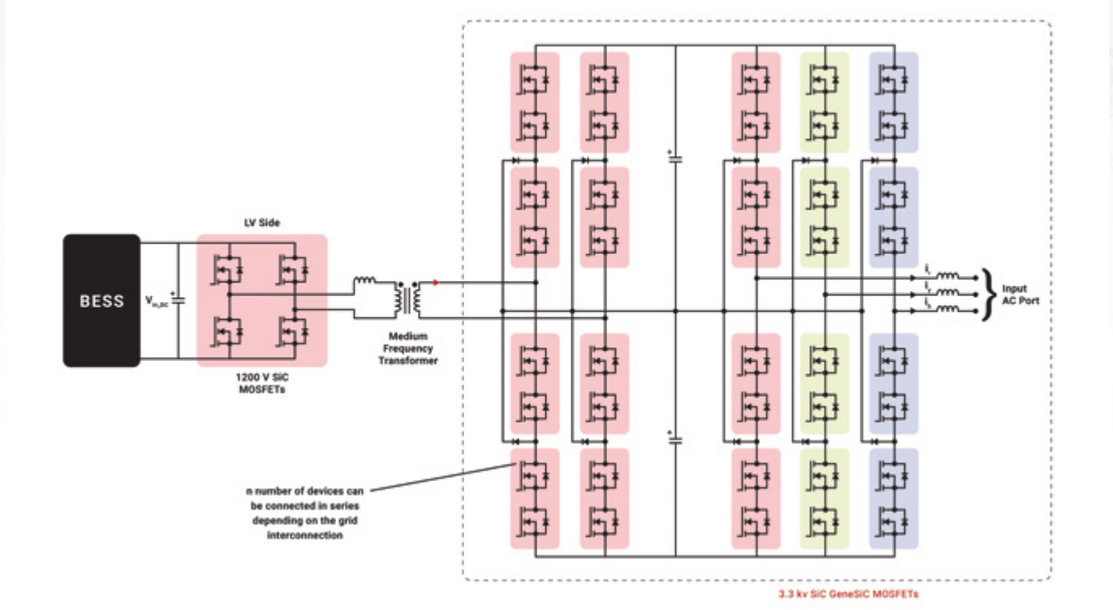


Figure 2: System topology for interconnecting the BESS system to an MV grid

requirement for a very low isolation capacitance in the gate-drive circuit. Power transmission stage design objectives are high isolation requirements, low coupling capacitance and optimized gate-driver footprint. In general, MV applications require series connection of devices for redundancy and high operating voltages. Series connection of MV SiC devices requires gate drivers that can switch all devices simultaneously. Delay in turn-on of the series-connected devices may result in voltage mismatch, leading to overvoltage or improper voltage sharing across devices.

Using MV 3.3-kV SiC MOSFET diodes in place of series-connected lower-voltage (1,200 V or 1,700 V) MOSFETs or IGBTs has tremendous advantages, including simpler gate driving, reduced parasitic inductance associated with replacing multiple lower-voltage transistors and rectifiers with a single MV device, lower conduction losses and higher efficiency. Overall size, weight and cooling requirements of the power converter can therefore be significantly reduced.

Tests of circuit efficiency and maximum junction temperatures on a 3.3-kV/400-A GeneSiC SiC MOSFET,

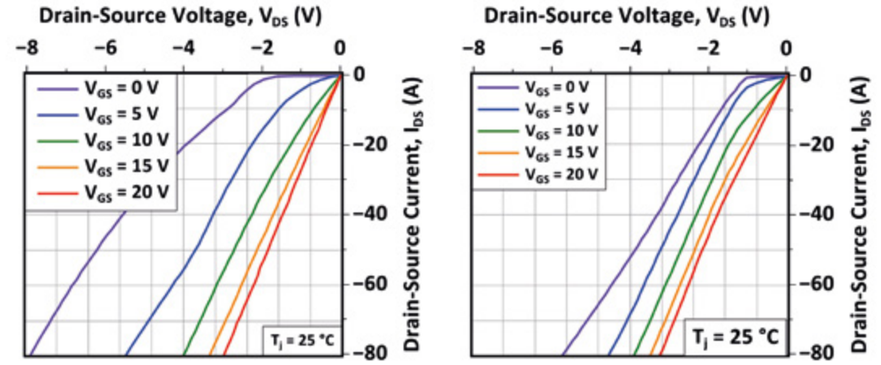


Figure 3: Third-quadrant I-V characteristics measured on 3.3-kV, 40-mΩ, discrete SiC MOSFET (left) and SiC MOSFET with monolithically integrated MPS diode (right)

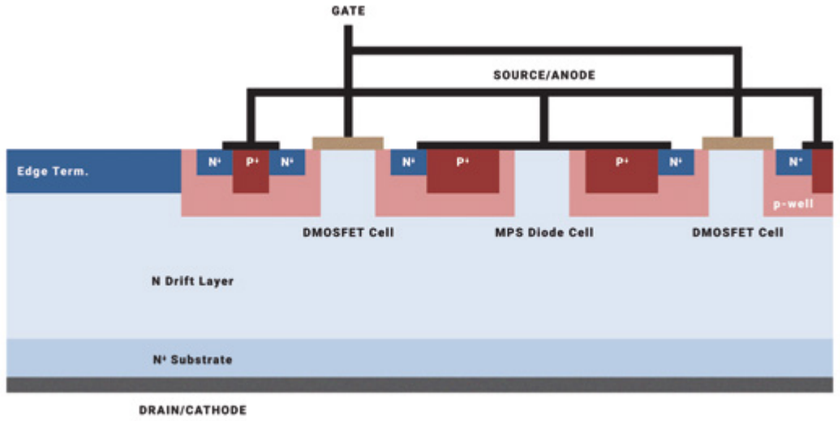


Figure 4: Cross-sectional device schematic of 3.3-kV SiC MOSFET with monolithically integrated Schottky rectifier

3.3-kV/400-A silicon IGBT and a series connection of two 1.7-kV/325-A SiC MOSFETs from a third party in a 4.16-kV modular multi-level converter have revealed significant benefits of the 3.3-kV SiC MOSFETs in MV applications. In general, the 3.3-kV SiC MOSFETs reduced semiconductor losses and supported a smaller installed semiconductor die area, improving the power density of the system (including volume of heatsinks and fans).

3.3-KV SiC MOSFET WITH MONOLITHICALLY INTEGRATED MPS DIODE

Further efficiency and reliability advantages can be achieved by monolithically integrating a merged PiN Schottky (MPS) diode within the MOSFET. This enables low conduction and switching-loss freewheeling diode operation without an externally connected Schottky diode while reducing the parasitic inductance associated with an external diode connection. Furthermore, this bypasses the built-in P-well/N-drift body diode of the D-MOSFET structure whose operation can induce faulting of the basal-plane dislocations inevitably present within the N-drift layer of the D-MOSFET.

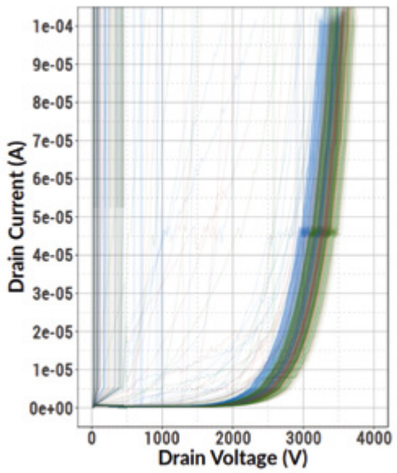


Figure 5: Third-quadrant breakdown characteristic measured on 3.3-kV SiC MOSFETs with monolithically integrated MPS diodes

Advantages include more efficient bidirectional performance, temperature-independent switching, low switching and conduction losses, reduced cooling requirements, superior long-term reliability, ease of paralleling and lower costs.

Navitas GeneSiC 3.3-kV discrete SiC MOSFETs and SiC MOSFETs with monolithically integrated MPS diodes typically have a breakdown-voltage range of 3,600–3,900 V, well above the datasheet value. When implementing a monolithic diode, there is a slightly higher drain-leakage current observed at elevated voltages, due to the Schottky barrier lowering under high electric fields. Figure 5 shows that in tests, GeneSiC mono-SiC MOSFETs demonstrated breakdown voltages in a range of 3.5 to 3.7 kV with leakages ≈ 50 µA (or 0.3 mA/cm^2) at the rated 3.3-kV blocking voltage, for an $R_{DS(on)}$ of approximately 80 mΩ (measured).

Unclamped inductive switching (UIS) measurements were used to investigate avalanche robustness of the 3,300-V SiC MOSFETs with integrated MPS diodes. The drain-current/-voltage waveforms at a peak drain current of 30 A are shown in Figure 6. Drain voltage rises to a maximum of 4,200 V during the test, and a maximum avalanche withstand time (t_{AV}) of 35 µs and single-pulse avalanche energy (E_{AS}) of 2.6 J (or 7.6 J/cm^2) are extracted from the UIS measurements. In comparison, the test performed on a discrete 3,300-V discrete SiC MOSFET with the same load inductance extracted an E_{AS} of 4.8 J.

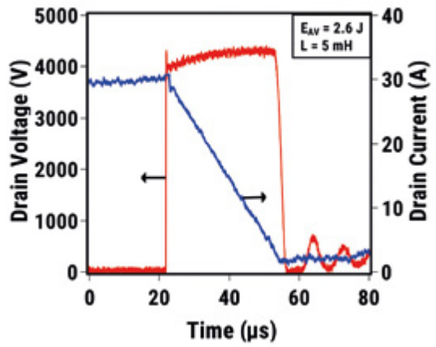


Figure 6: Drain-current and drain-voltage waveforms from UIS measurement performed on a 3.3-kV SiC MOSFET with monolithically integrated MPS diode

SHORT-CIRCUIT ROBUSTNESS

The short-circuit robustness of the GeneSiC MOSFETs was evaluated by subjecting 3.3-kV discrete SiC MOSFETs with and without monolithically integrated MPS diodes to a 1,200-V DC-link. A 20-V/–5-V gate-drive scheme was used and the device was mounted on a 25°C baseplate. The drain current increases to a maximum of 525 A during the short-circuit pulse and a short-circuit withstand time of 4.5 µs was measured (Figure 7).

SUMMARY

Deploying SiC in inverters will accelerate the adoption of energy storage technologies and make them critical elements of future grids. Integrating a BESS to an MV grid through an isolated topology shows that using 3.3-kV single SIC MOSFETs enables higher system efficiency, lower operating temperature and smallest die size, compared with an equivalent silicon IGBT or two 1,700-V SiC MOSFETs in series.

GeneSiC 3.3-kV SiC MOSFETs with monolithically integrated monolithic MPS diodes achieve breakdown voltages well above 3.3 kV and demonstrate smooth switching performance while fully activating the monolithic MPS diode. This significantly reduces power losses in third-quadrant operation and enhances device reliability by alleviating bipolar degradation. UIS testing reveals a robust avalanche capability and short-circuit withstand times to 4.5 µs.

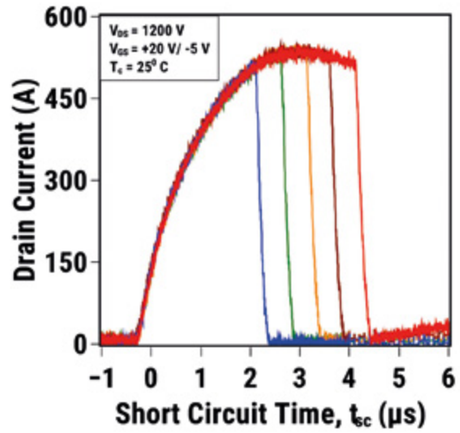


Figure 7: Drain-current waveform recorded during a short-circuit test performed on a 3,300-V SiC MOSFET with monolithically integrated MPS diode at a DC-link voltage of 1,200 V

Reference

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NEWS

NEWS

Infineon Bolsters Its GaN Market with Acquisition

Infineon and GaN Systems are joining forces.

GaN Systems and Infineon Technologies announced that they have signed a legally binding agreement under which Infineon would purchase GaN Systems for $830 million. This deal will significantly strengthen Infineon's gallium nitride activities, the business ownership of which is with the Power Systems division. The acquisition is still subject to customary regulatory approvals and closing conditions. During the announcement, Adam White and Ulrich Pelzer, president and CFO, respectively, of Infineon's Power & Sensor Systems (PSS) Division, said that this transaction will strengthen Infineon's portfolio and leadership in power systems.

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